ROBERT R. McCORMICK SCHOOL OF ENGINEERING AND APPLIED SCIENCE

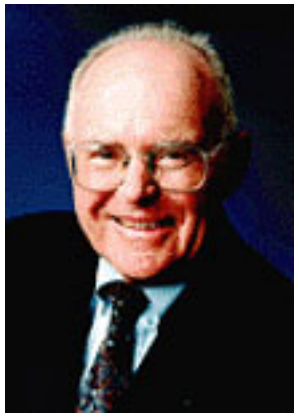
Nanoelectronics: Device Physics and Fabrication Technology

Mark C. Hersam
Professor

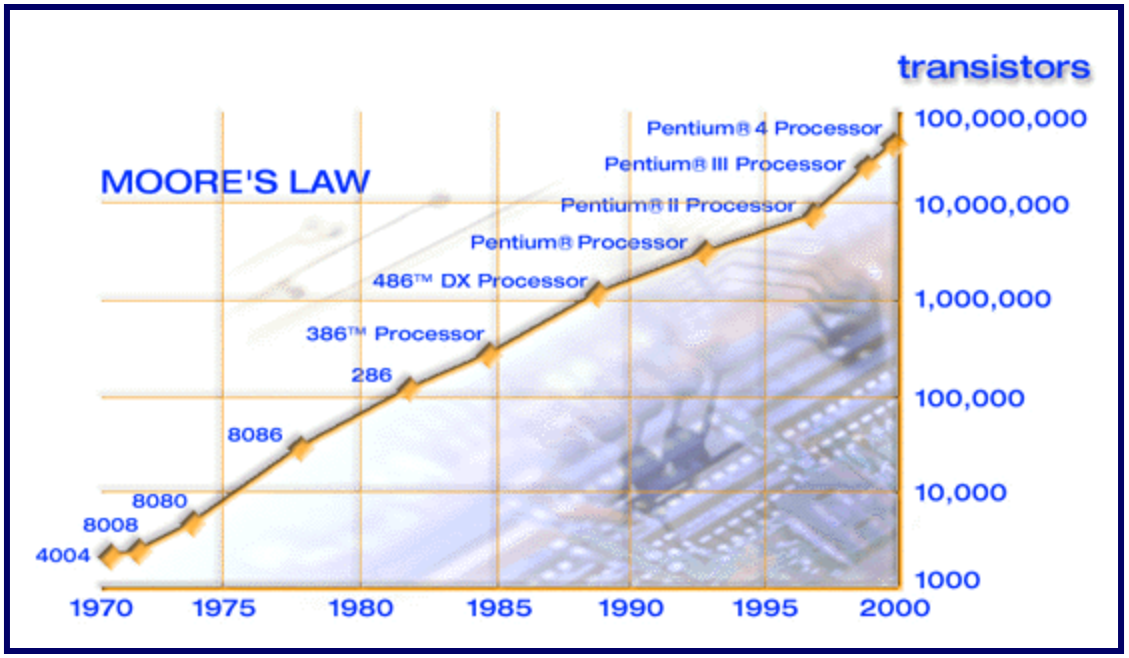
Department of Materials Science and Engineering
Northwestern University, Evanston, IL 60208-3108
Ph: 847-491-2696, m-hersam@northwestern.edu
http://www.hersam-group.northwestern.edu/

"640K ought to be enough for anybody"
- Bill Gates, 1981

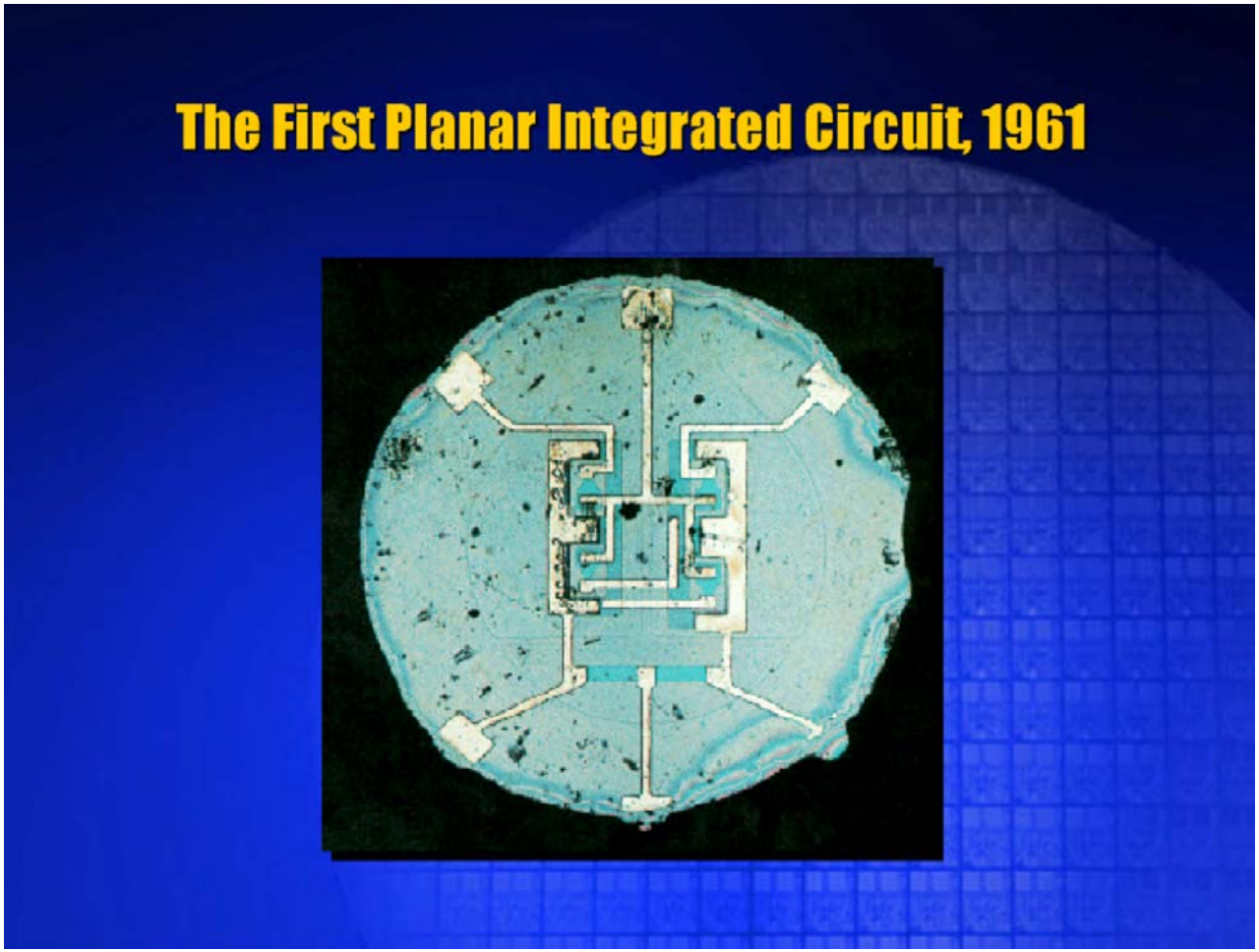
Moore's Law



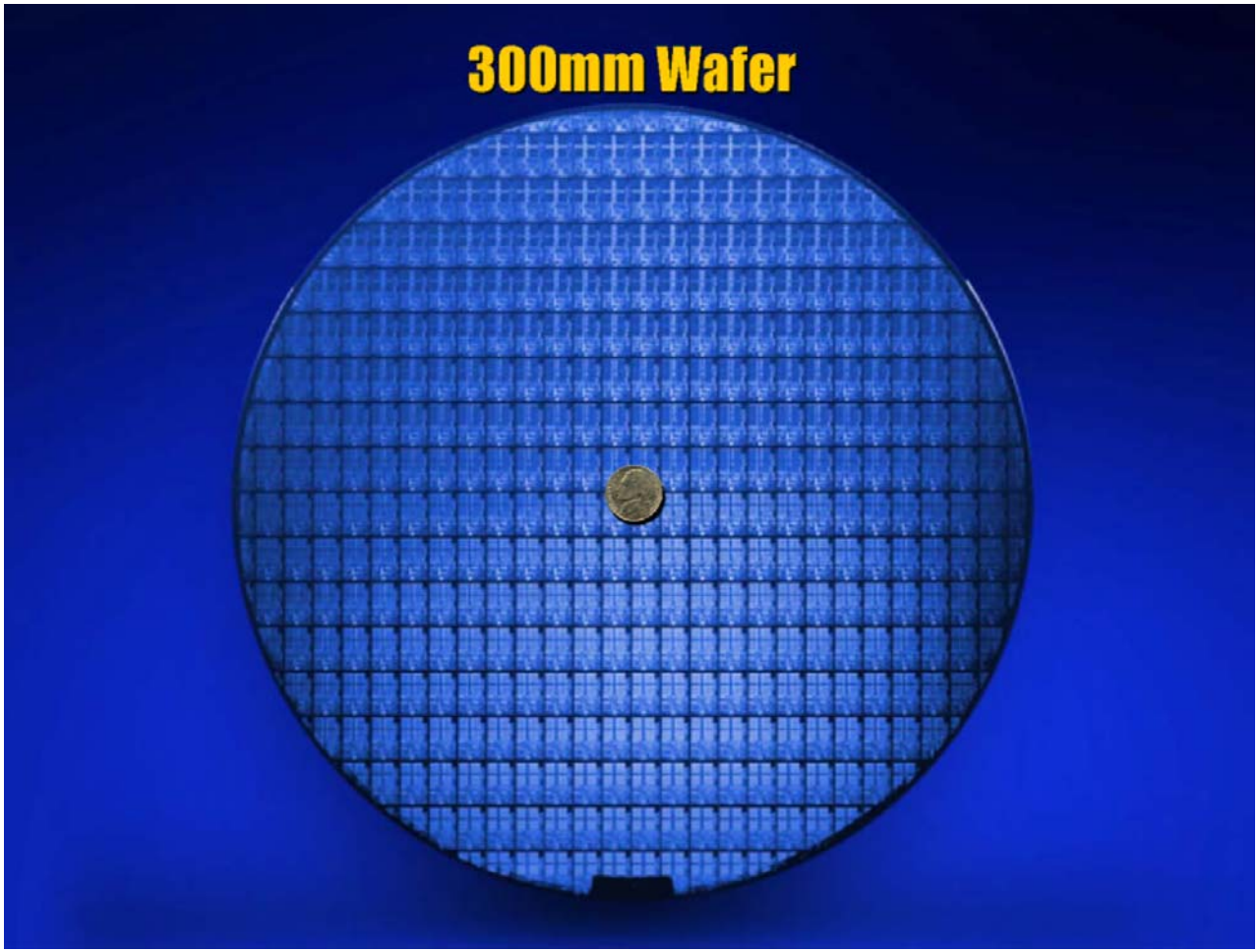
Intel Co-Founder
Gordon E. Moore



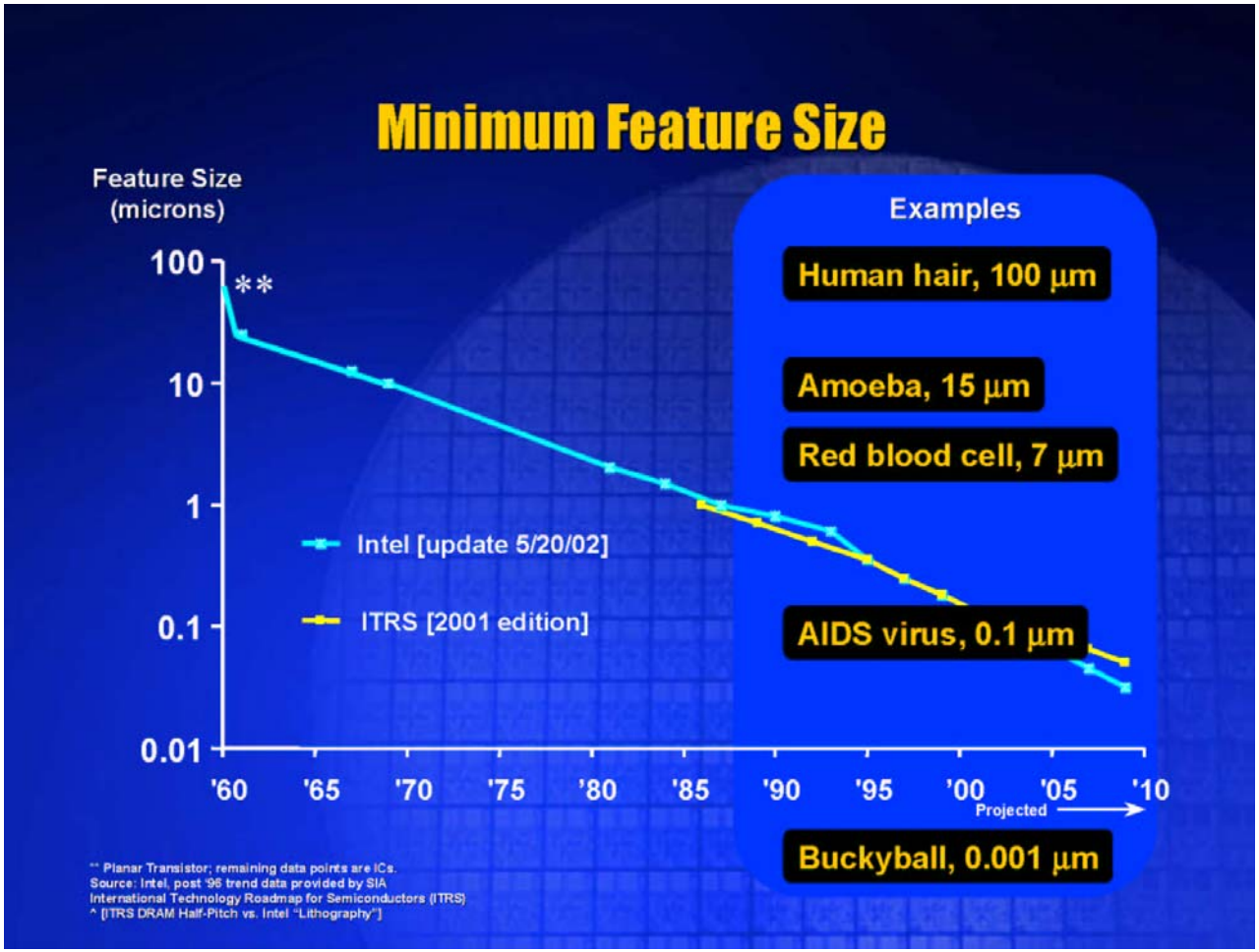
"Cramming More Components Onto Integrated Circuits"
Author: Gordon E. Moore
Publication: Electronics, April 19, 1965



"No Exponential is Forever … but We Can Delay 'Forever',"
Gordon E. Moore, International Solid State Circuits Conference, Feb. 10, 2003.

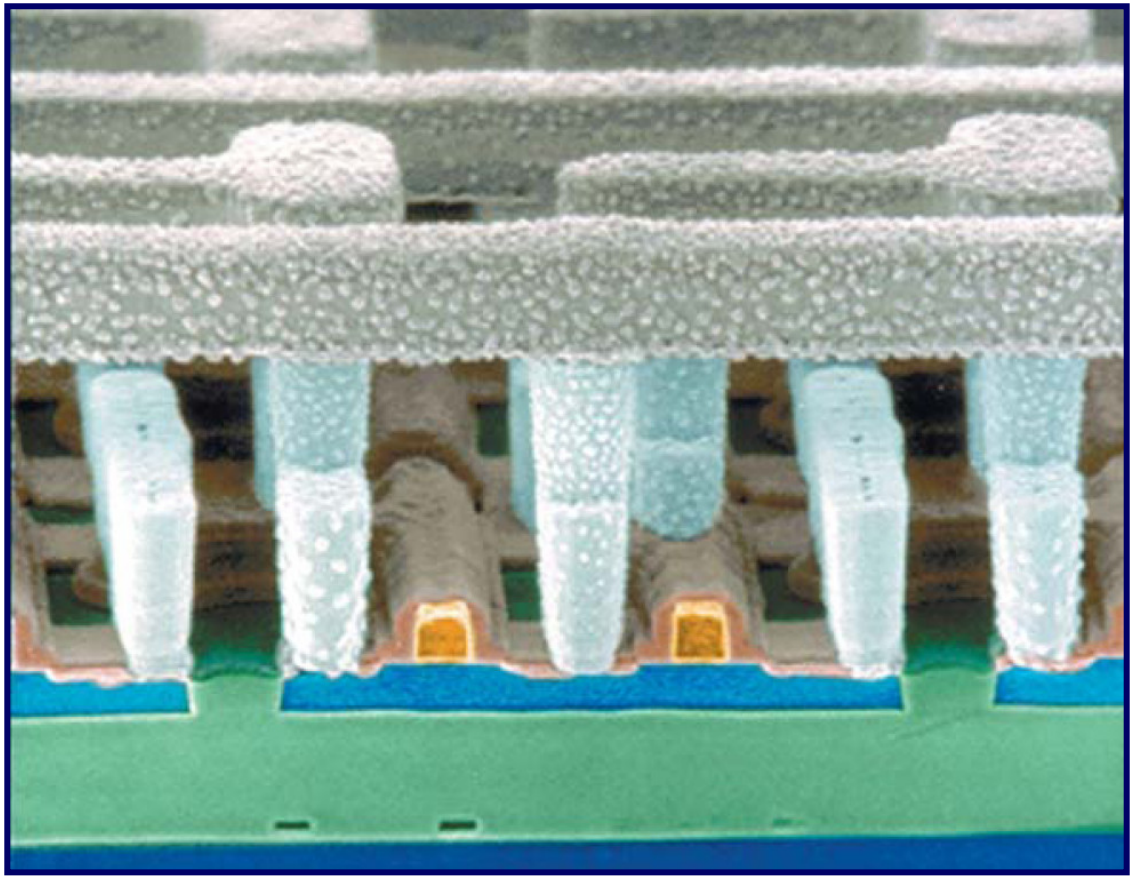


"No Exponential is Forever … but We Can Delay 'Forever',"
Gordon E. Moore, International Solid State Circuits Conference, Feb. 10, 2003.



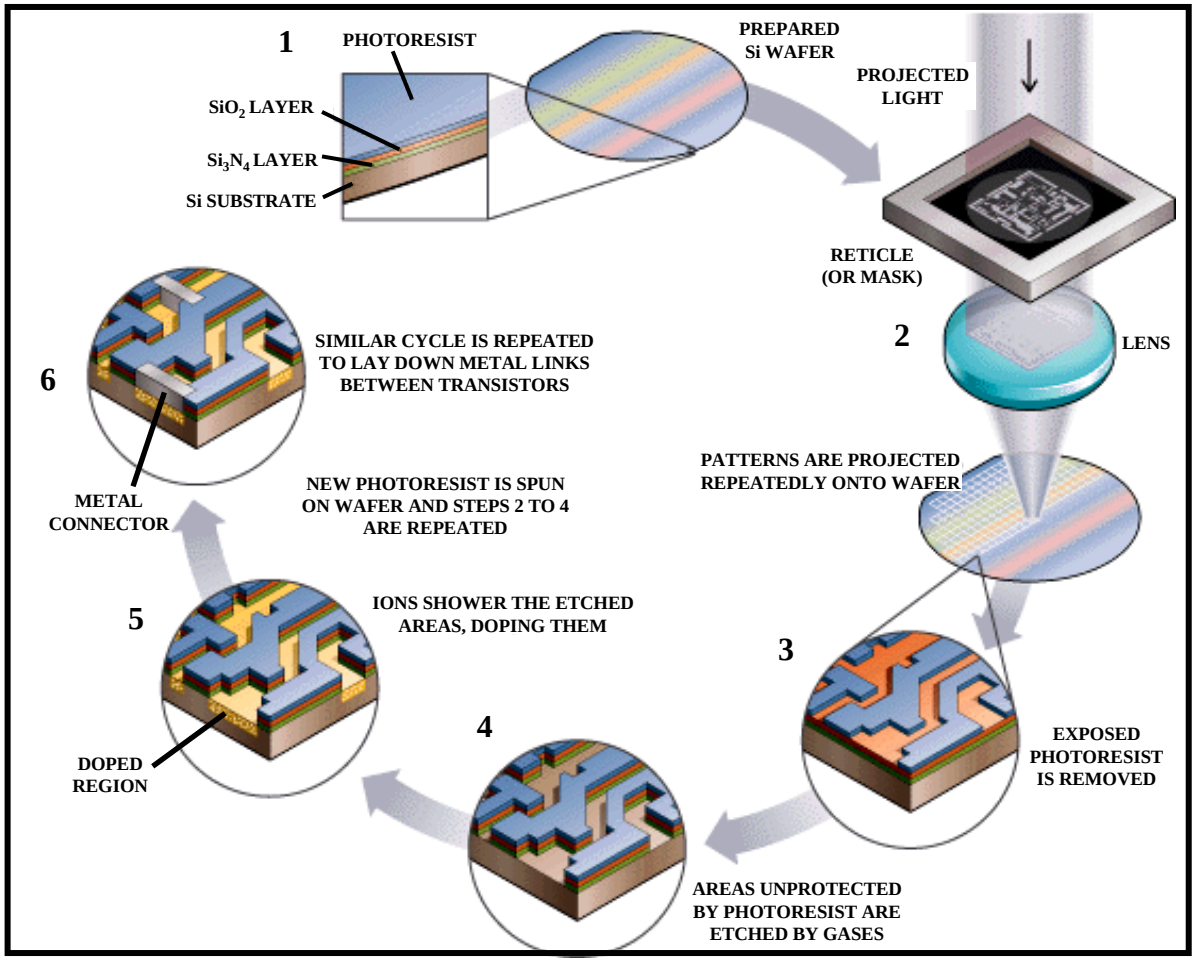
"No Exponential is Forever … but We Can Delay 'Forever',"
Gordon E. Moore, International Solid State Circuits Conference, Feb. 10, 2003.

IC Manufacturing Approach: Lithography



G. D. Hutcheson, *et al.*, *Scientific American*, **290**, 76 (2004).

Typical Lithographic Process Flow



G. D. Hutcheson, *et al.*, *Scientific American*, **274**, 54 (1996).

Lithography Yield

NOTE: Typical fabrication facilities (fabs) have product yields > 95%

→ Lithography yield per step > 99%

Lithography is 90% of the production cost in modern day fabs

G. Timp, *Nanotechnology*, Chapter 4

Lithography Areal Throughput

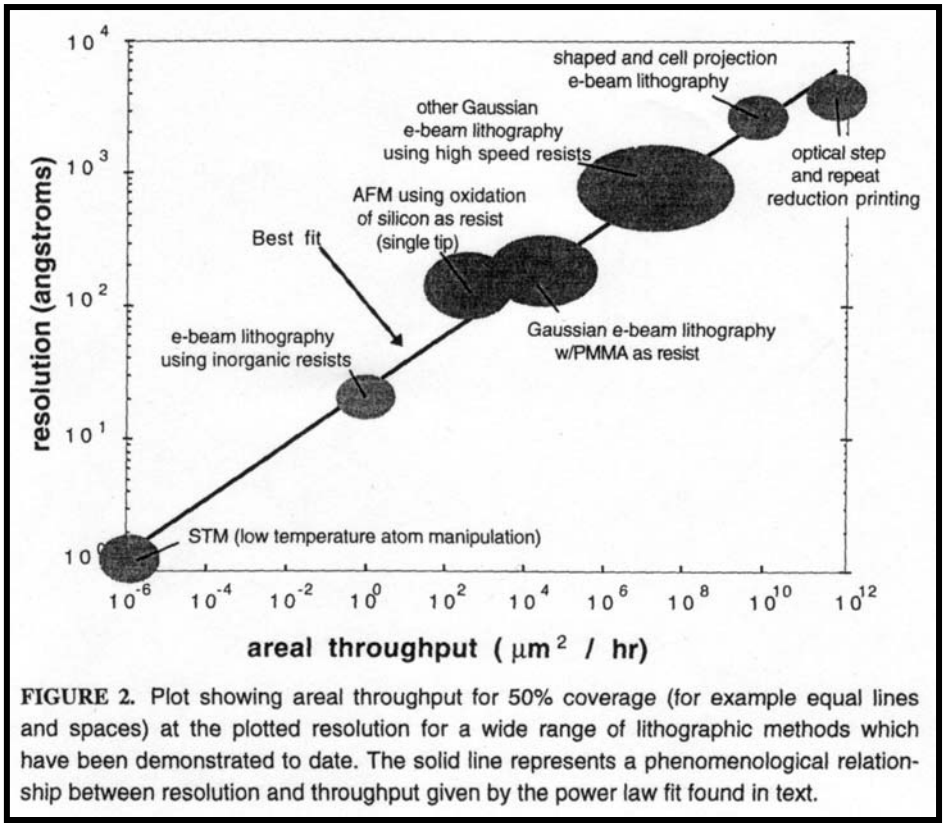


FIGURE 2. Plot showing areal throughput for 50% coverage (for example equal lines and spaces) at the plotted resolution for a wide range of lithographic methods which have been demonstrated to date. The solid line represents a phenomenological relationship between resolution and throughput given by the power law fit found in text.

Phenomenological Relationship:

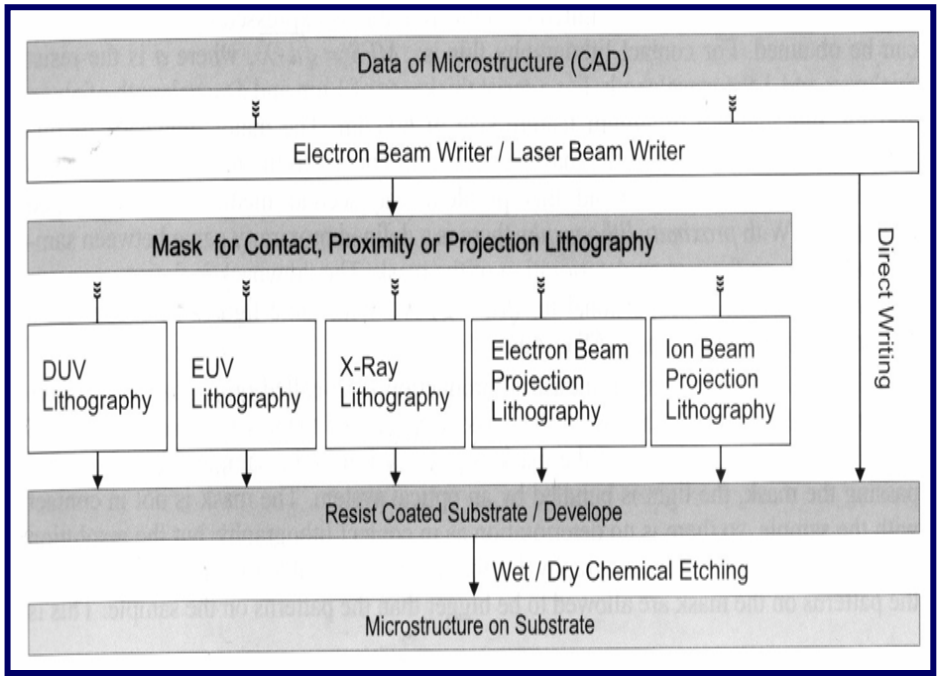
$$\text{Resolution (Å)} \sim 23 A_t^{0.2}$$

(A_t = areal throughput in $\mu m^2/hr$)

This phenomenological relationship is essentially true over **18 orders of magnitude** in throughput!

G. Timp, *Nanotechnology*, Chapter 4

Lithography Pathways



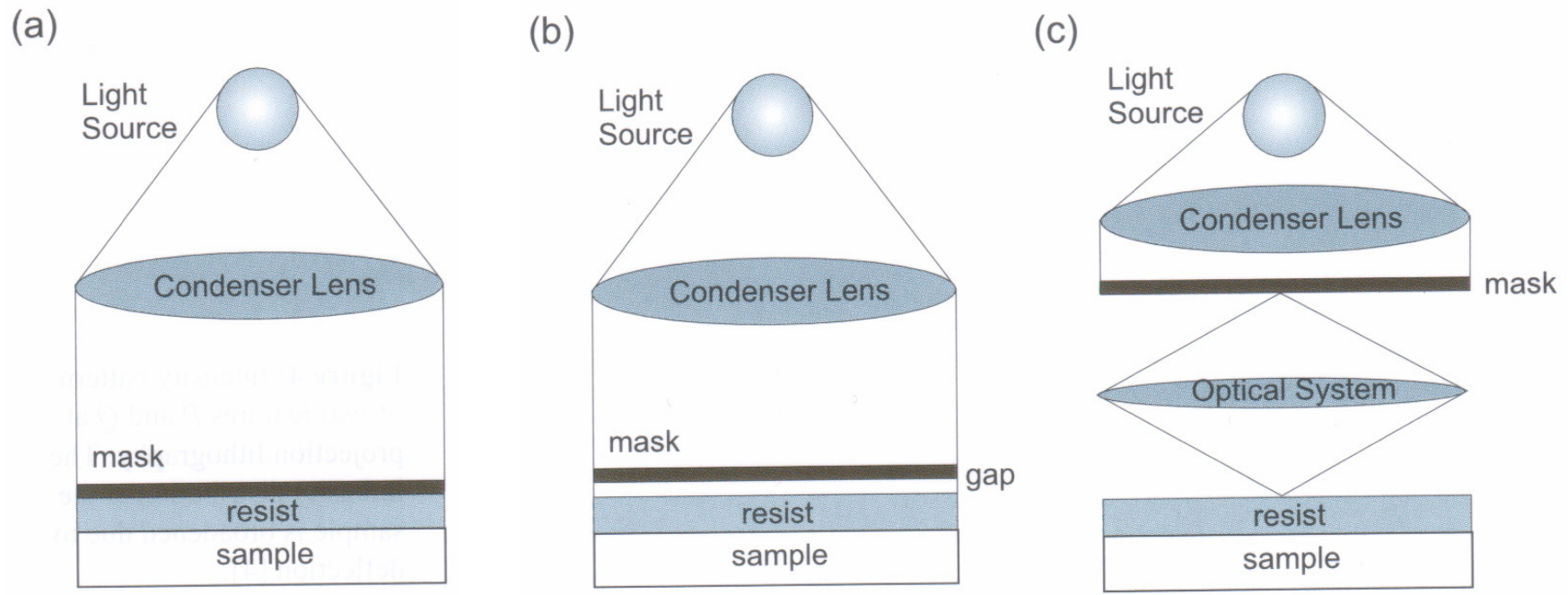
Pathways from pattern design to pattern transfer:

(1) Can be direct (e.g., e-beam or ion beam lithography)

(2) Usually a 2 step process
  (A) Generation of mask
  (B) Transfer of its pattern to a large number of substrates

R. Waser (ed.), *Nanoelectronics and Information Technology*, Chapter 9

Masking Methods



Contact **Proximity** **Projection**

R. Waser (ed.), *Nanoelectronics and Information Technology*, Chapter 9

Limitations of Optical Lithography

Minimum feature size = $k\lambda$/NA

where k = proportionality factor
(typically 0.5 for diffraction limited systems)
λ = wavelength
NA = numerical aperture = sin α
(2α = acceptance angle of lens at point of focus)
→ measure of light gathering power of lens

However, depth of focus = $\lambda/(\text{NA})^2$
→ important because wafers are not flat

Increasing NA is not the answer → reduce λ to reduce feature size

Deep Ultra-Violet Lithography

Deep UV → Excimer Laser Sources:

XeF → 351 nm

XeCl → 308 nm

KrF → 248 nm

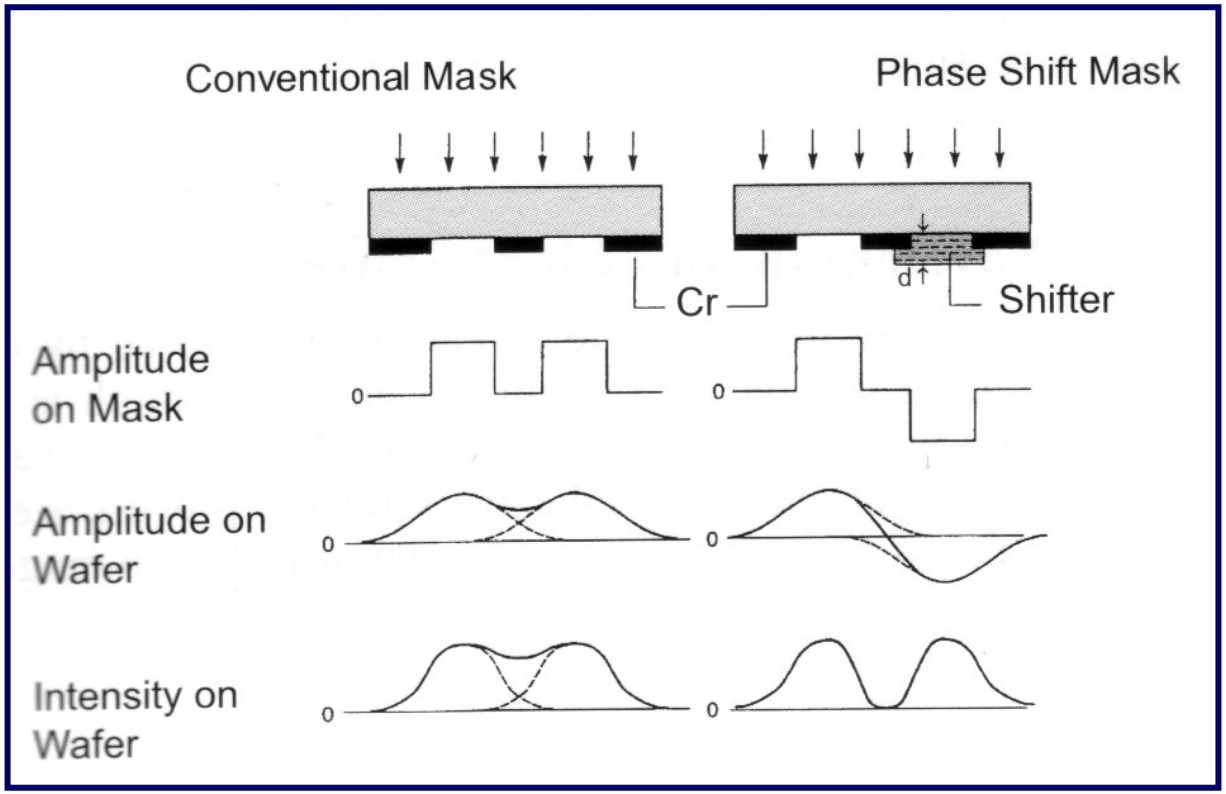
} Fused silica / quartz optics

ArF → 193 nm

F_2 → 157 nm

} CaF optics → difficult to grind and polish due to hygroscopic (water-absorbing) properties

Phase Shifting Masks



→ Minimizes diffraction effects but complicates mask making

R. Waser (ed.), *Nanoelectronics and Information Technology*, Chapter 9

Extreme Ultra-violet Lithography

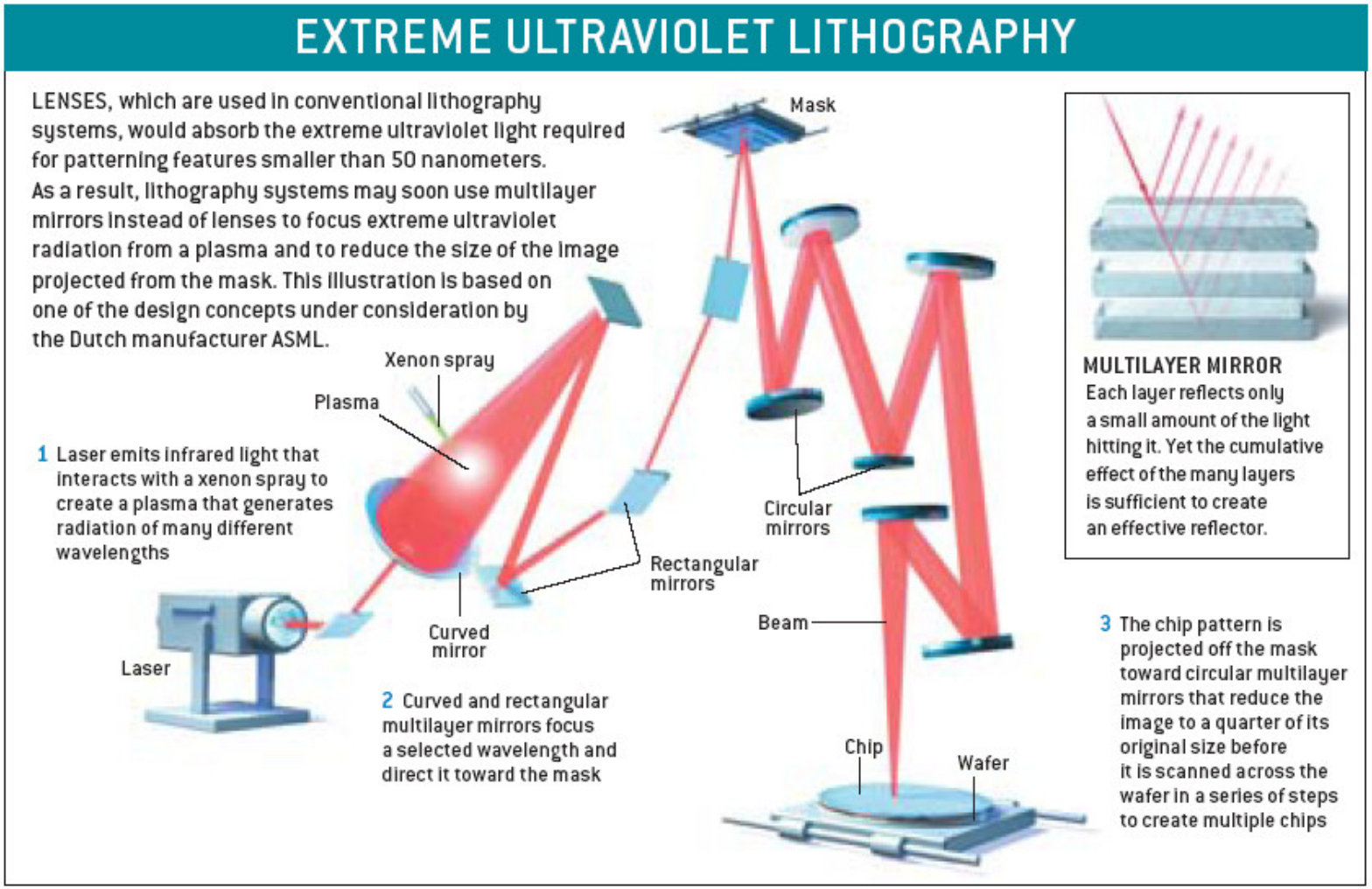
(a.k.a., soft x-ray lithography)

- Developed at Sandia National Laboratory in 1996
- EUV source based on a plasma created when a laser is focused on a beam of Xe gas clusters expanding at supersonic speeds
- $\lambda \sim 10$ nm

NOTE: At short λ, optical materials are highly absorptive

→ Reflective optics (e.g., Bragg reflectors)
→ Thin, defect-free masks

e.g., at $\lambda = 13$ nm, reflector consists of 40 layer pairs of Mo and Si with 7 nm periodicity per layer pair



G. D. Hutcheson, *et al.*, *Scientific American*, **290**, 76 (2004).

Depth of focus is less of an issue at short wavelengths

→ high aspect ratio resist profiles are possible with EUV

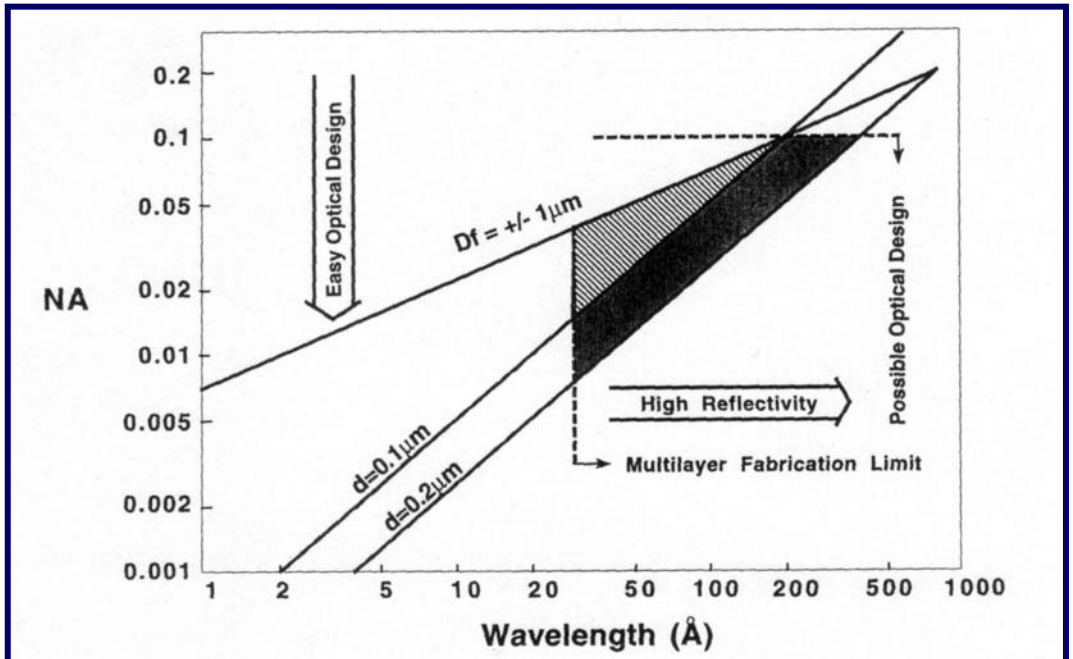


FIGURE 16. Sets of numerical aperture and EUV wavelengths capable of meeting the diffraction limited resolution and depth of focus requirements of a projection camera design. The shaded regions correspond to a bound of ± 1 μm of DOF and two different resolutions, $d = 0.2$ and $d = 0.1$ μm[70].

G. Timp, *Nanotechnology*, Chapter 4

Example of resist patterned with EUV lithography:

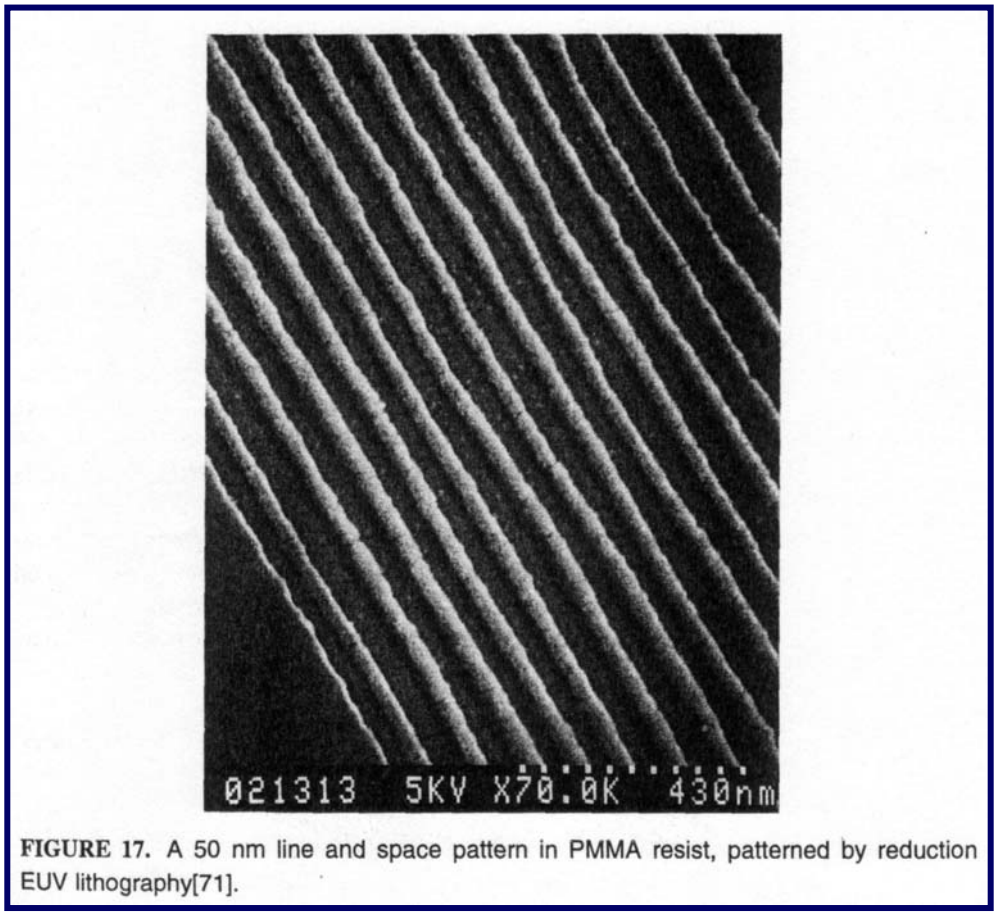


FIGURE 17. A 50 nm line and space pattern in PMMA resist, patterned by reduction EUV lithography[71].

G. Timp, *Nanotechnology*, Chapter 4

X-Ray Lithography

- λ = 1 nm BUT resolution = $k(\lambda g)^{1/2}$

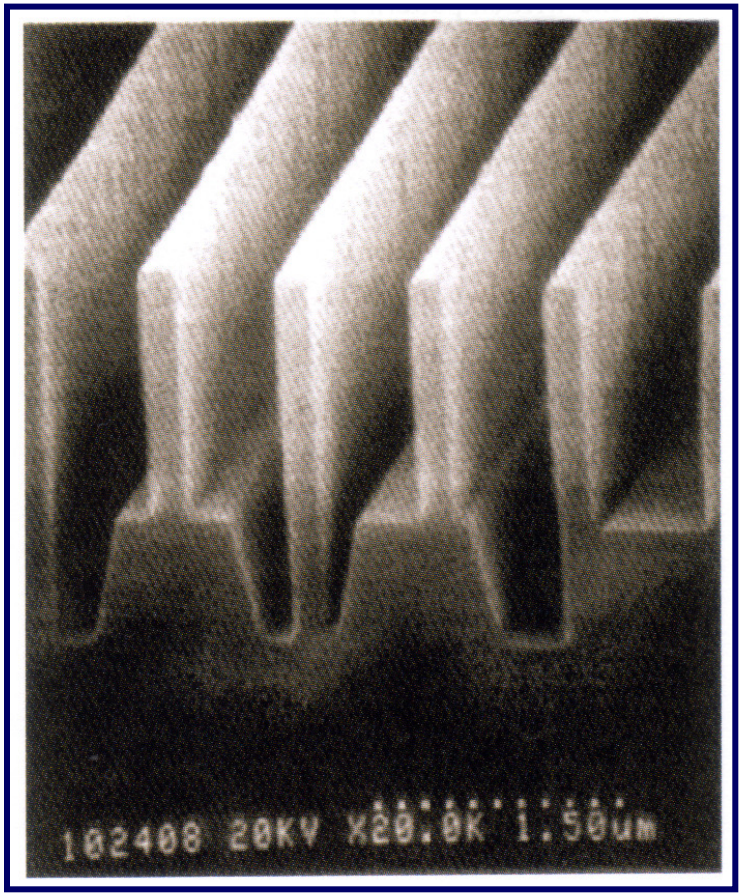
  where g = size of gap between mask and substrate
  (tends to be 5 – 40 μm in production)

- Therefore, resolution = 0.07 – 0.2 μm for λ = 1 nm

- However, when contact printing is done in research environments, 30 nm resolution is achievable

- High aspect ratios are achieved in developed resists

Example of resist patterned with x-ray lithography:



R. Waser (ed.), *Nanoelectronics and Information Technology*, Chapter 9

Established Advantages of X-Ray Lithography

(1) Large depth of focus

(2) Excellent resist profiles (pillars of resist)

(3) Large process latitude

(4) Linewidth independent of substrate topography or type

(5) Relatively immune to low atomic weight contaminants

Remaining Disadvantages of X-Ray Lithography

(1) 1X mask technology (gold on 1 – 2 μm thick silicon)
→ Defects, aspect ratio, bending, and heating are problems
(2) Source cost and/or complexity
(3) Alignment/registration is nontrivial

To become a commercial success, x-ray lithography needs:

(A) A mask → distortion free, inspectable, repairable
(B) A resist → presently acceptable but could be improved
(C) An alignment/registration system
(D) An x-ray source → acceptable cost and throughput

Ion Beam Lithography

- Typically, liquid metal (e.g., gallium) ions are used
- Ion projection lithography developed in the late 1970's
- Advanced lithography group → consortium of industry, government, and universities
- ALG-1000 → 20 μm by 20 μm fields at 3X reduction using 150 keV hydrogen ions → 0.1 μm resolution

Advantages of Ion Beam Lithography

(1) Less long range scattering than electrons

(2) Ion beams stay near initial trajectory
→ no dose adjustment for different patterns or substrates

(3) Can directly write metal lines (focused ion beam)
→ suitable for mask repair

Disadvantages of Ion Beam Lithography

(1) Ions interact strongly with target causing:
- (A) Ion mixing
- (B) Amorphizing crystals
- (C) Altered optical properties
- (D) Implanted dopants
- (E) Sputter etching

(2) Ions are highly absorbed (typically within 10 nm)
- → Stencil type masks
- → The center of a ring falls out unless sub-resolution supports are used

Electron Beam Lithography

- Very popular in research environments
- Used for mask making commercially
- $\lambda = h/(2mE)^{1/2}$ → λ = 7.7 pm @ 25 keV
- Typically, EBL is direct write → serial (slow) process
- Projection EBL systems have been developed
  → e.g., SCALPEL

(SCALPEL = Scattering with Angular Limitation Projection Electron-beam Lithography)

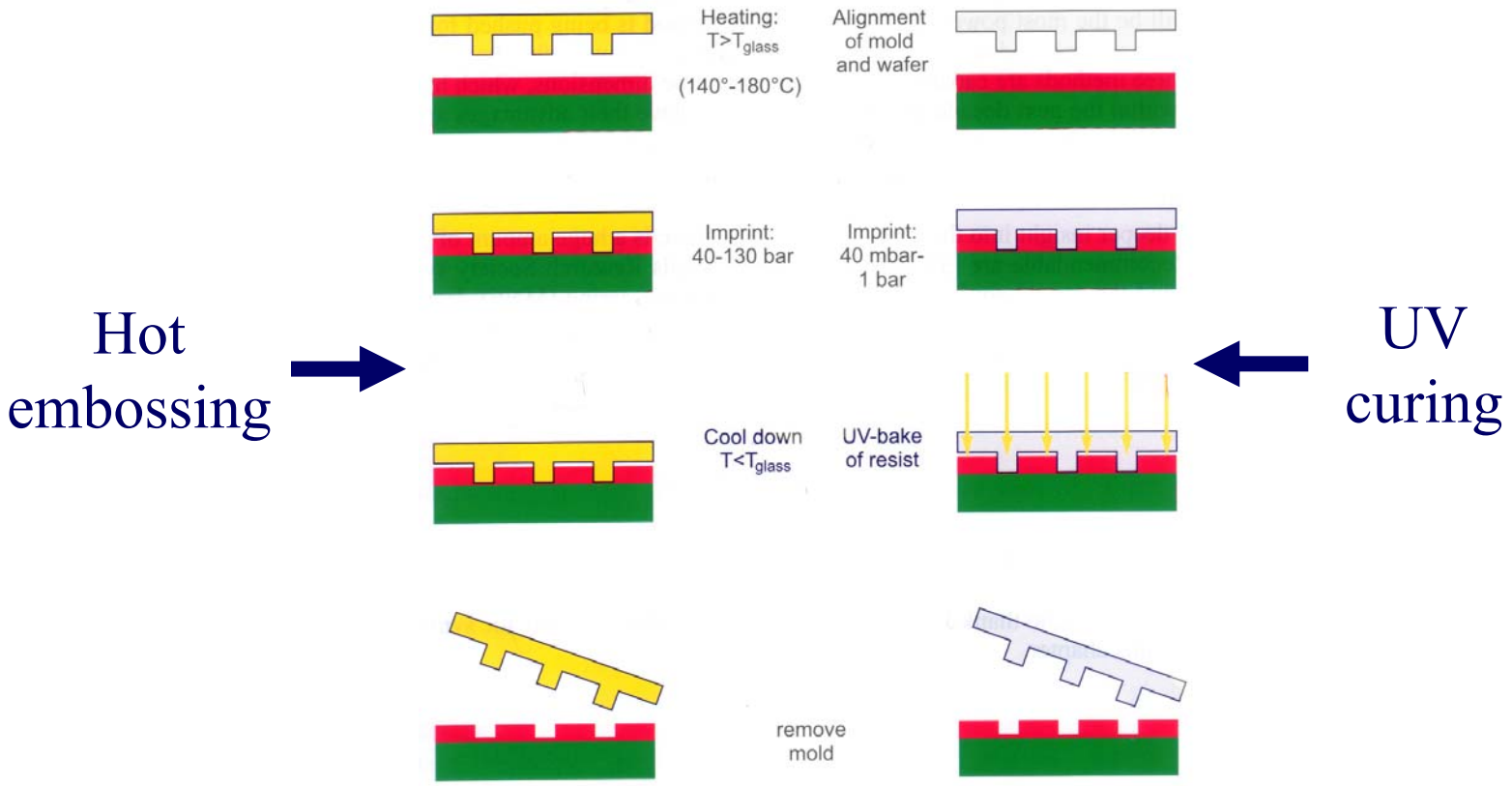
Advantages of Electron Beam Lithography

(1) High resolution → down to 5 nm
(2) Useful design tool → direct write allows for quick pattern changes (no masks are needed)

Disadvantages of Electron Beam Lithography

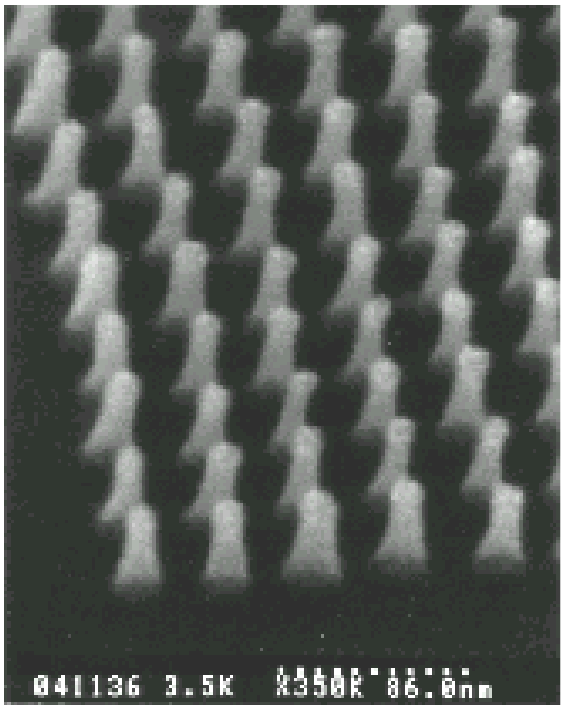
(1) Cost (up to $6 – 10 million for hardware)
(2) Direct write has low throughput → slow and expensive

Nanoimprint Lithography

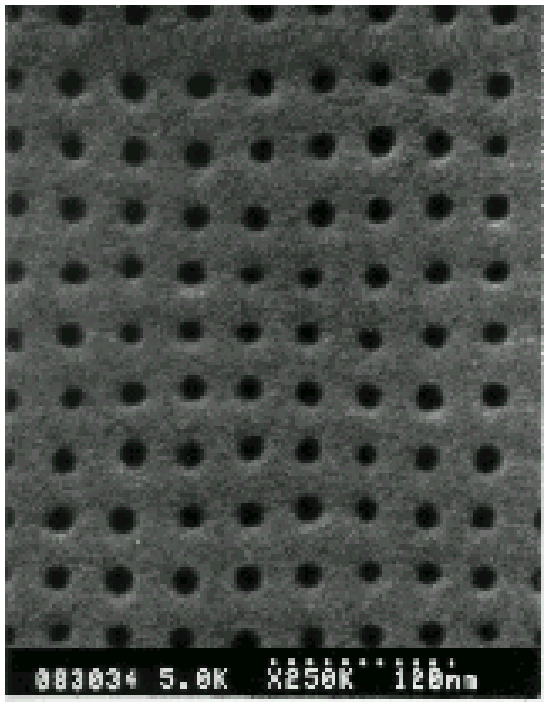


R. Waser (ed.), *Nanoelectronics and Information Technology*, Chapter 9

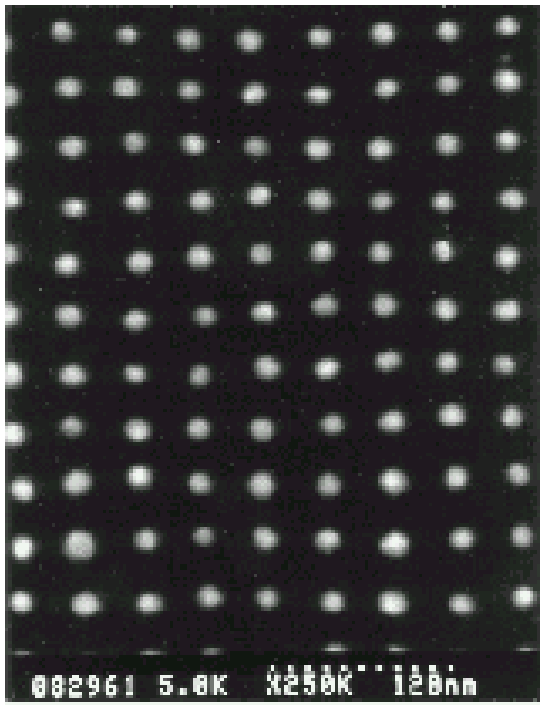
Nanoimprint Lithography Patterns



~20 nm pillars



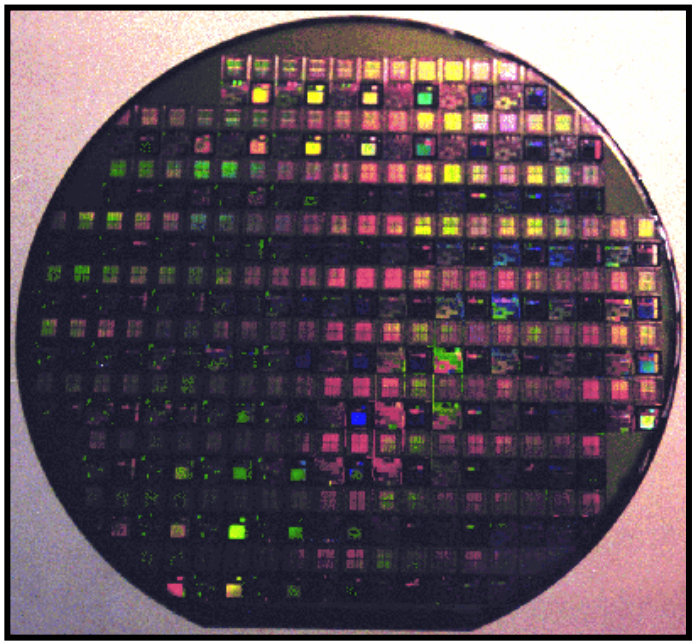
~20 nm holes

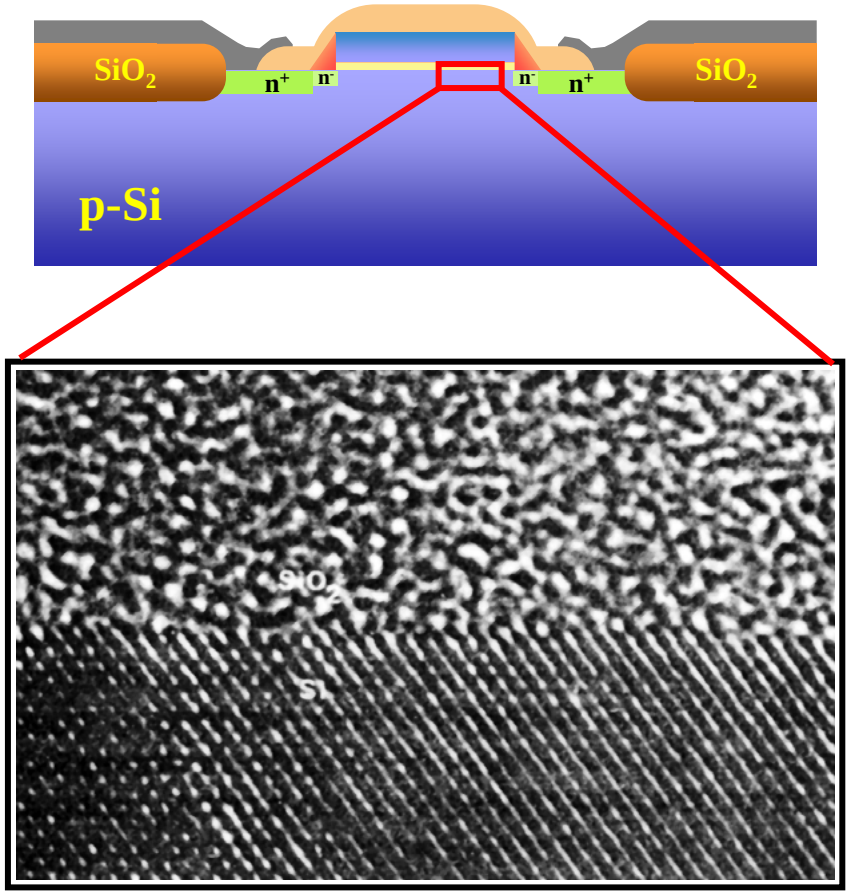


~20 nm dots

P. R. Krauss, *et al.*, *Appl. Phys. Lett.*, **71**, 3174 (1997).

Silicon MOSFET Geometry





MOSFET = Metal-Oxide-Semiconductor Field Effect Transistor

Complementary MOS (CMOS)

* Silicon is the most widely material for microprocessors and other logic circuitry because it can implement CMOS architectures

Simplest logic gate:
INVERTER

$V_{in} = V_{DD} \rightarrow V_{out} = 0$ V

$V_{in} = 0$ V $\rightarrow V_{out} = V_{DD}$

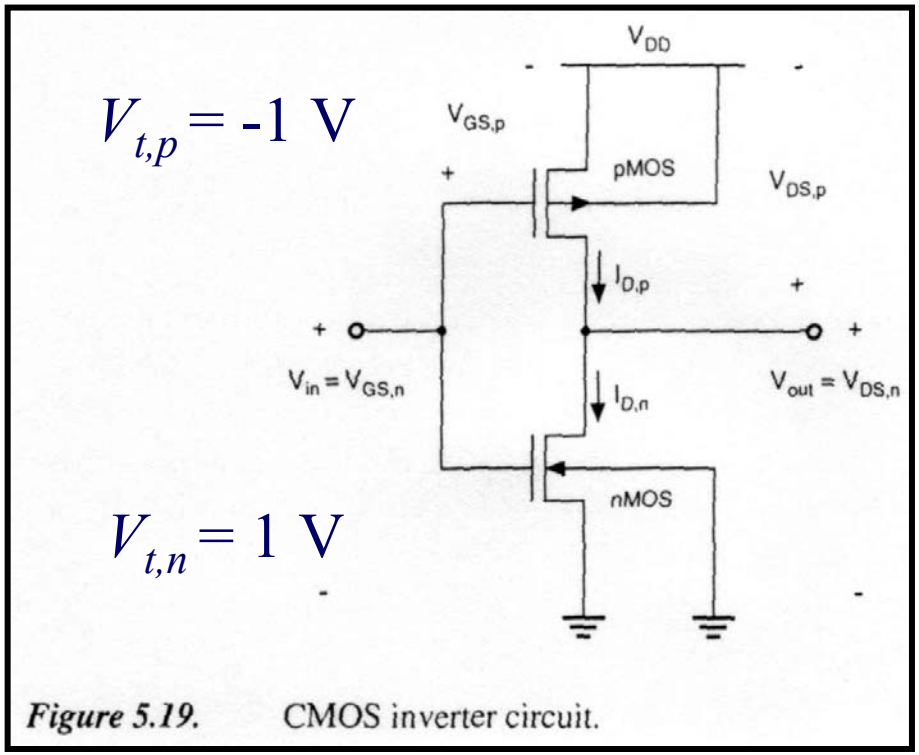


Figure 5.19. CMOS inverter circuit.

S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits*, McGraw-Hill Company (1996).

Why CMOS?

- In steady-state, there is no path from V_{DD} to ground
- Consequently, power is only dissipated during switching (Note: power dissipation increases with speed)
- Without CMOS, power is dissipated when input is high:

$$V_{in} = V_{DD} \rightarrow P = V_{DD}^2/R$$

Highly integrated logic circuits require CMOS

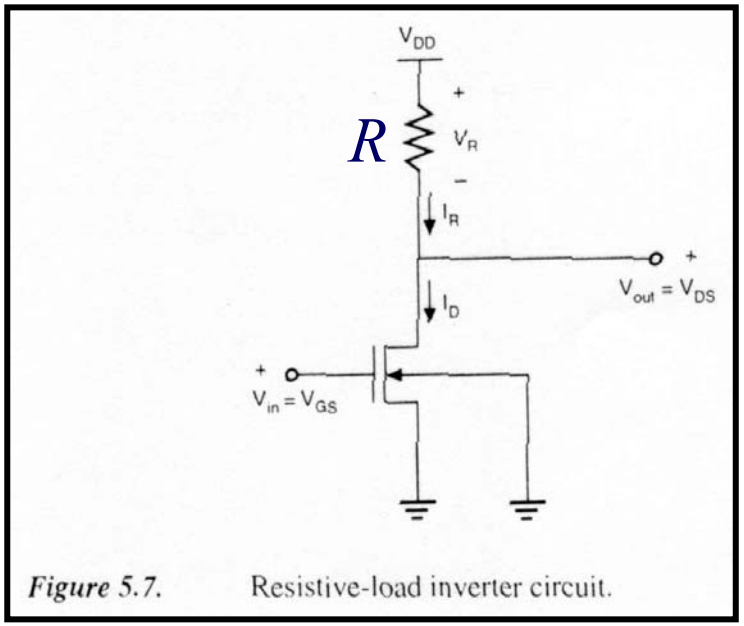


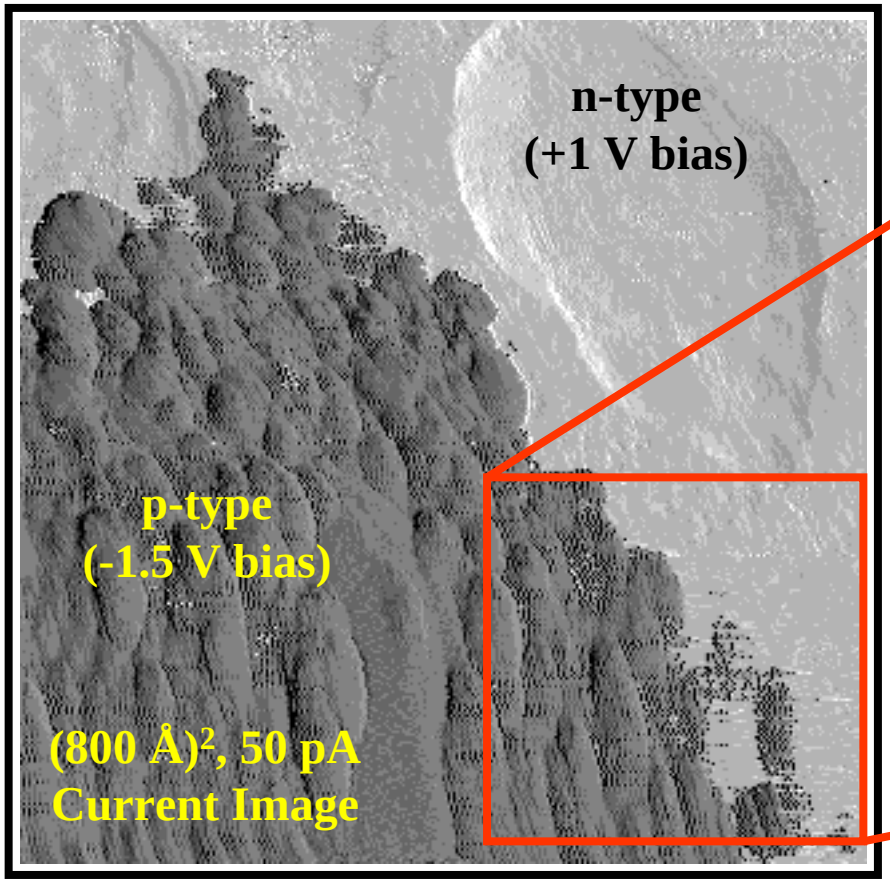
Figure 5.7. Resistive-load inverter circuit.

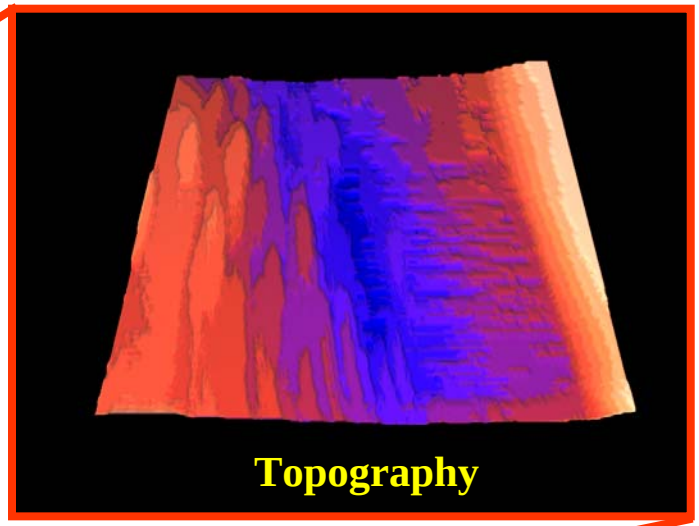
S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits*, McGraw-Hill Company (1996).

Limitations of CMOS at the Nanoscale

(1) Statistical variations in dopants:

Substrate: Si(100), p-type, B-doped (~ 0.01 Ω-cm)
Processing: 1.) Phos. predep @ 1000°C for 10 min.
2.) Phos. drive @ 1000°C for 10 min.
3.) ~ 1000°C anneal in UHV for 1 min.





Limitations of CMOS at the Nanoscale

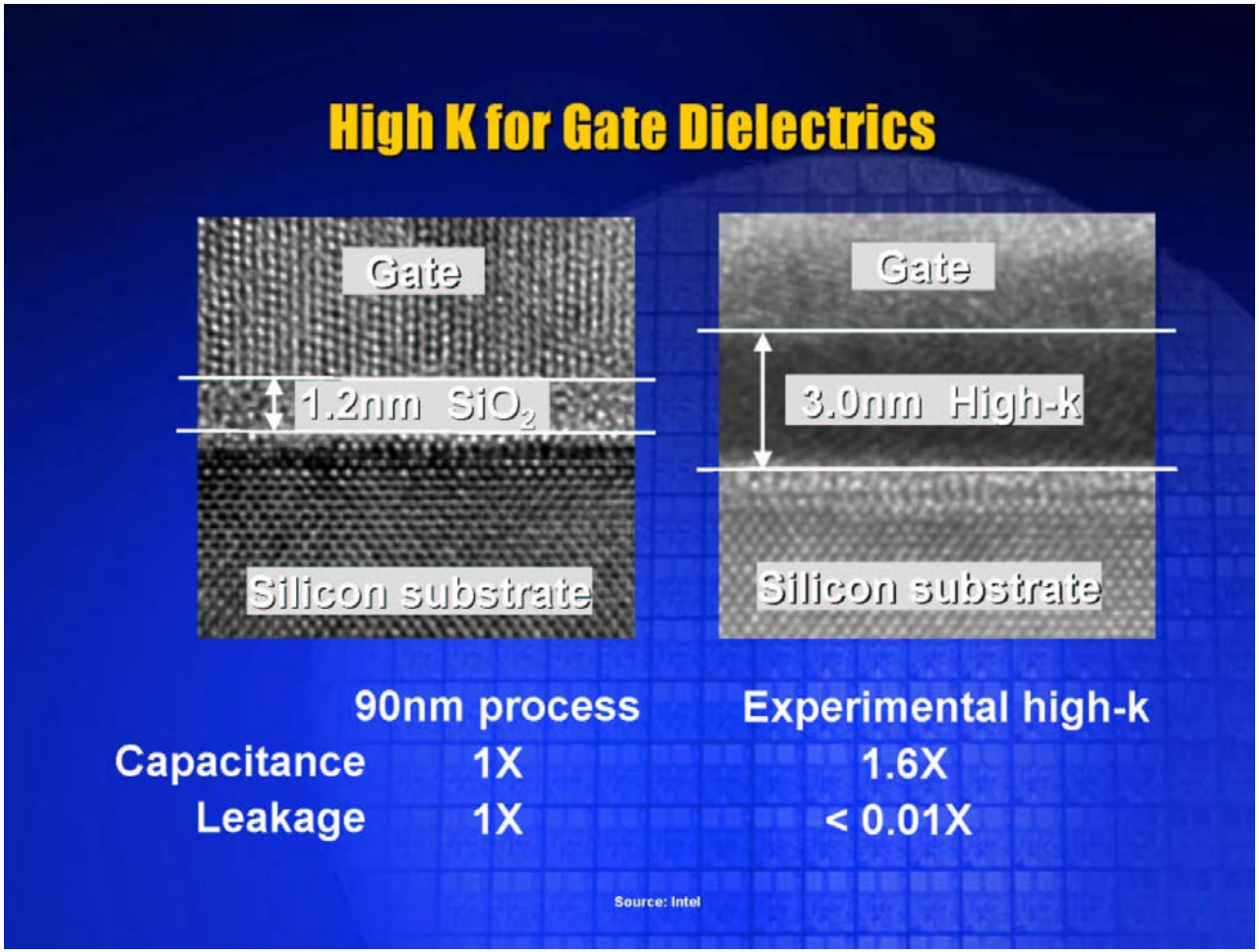
(2) Gate oxide scales with channel length

(At ~ 1 nm gate oxide thickness, large gate leakage current due to tunneling)

NOTE: $C_{ox} = \varepsilon_{ox} A / d_{ox}$

(Rather than decrease d_{ox}, increase ε_{ox})

→ High k dielectric materials



"No Exponential is Forever … but We Can Delay 'Forever',"
Gordon E. Moore, International Solid State Circuits Conference, Feb. 10, 2003.

Problems with High K Dielectrics

Two new interfaces:

(1) Interface between high k dielectric and silicon needs to be as free of dangling bonds as possible

(2) Interface between high k dielectric and poly silicon gate leads to two problems:

(a) Phonon scattering, which decreases speed

(b) Threshold voltage is pinned to high values

Integrating High K Dielectrics with Metal Gate Electrodes

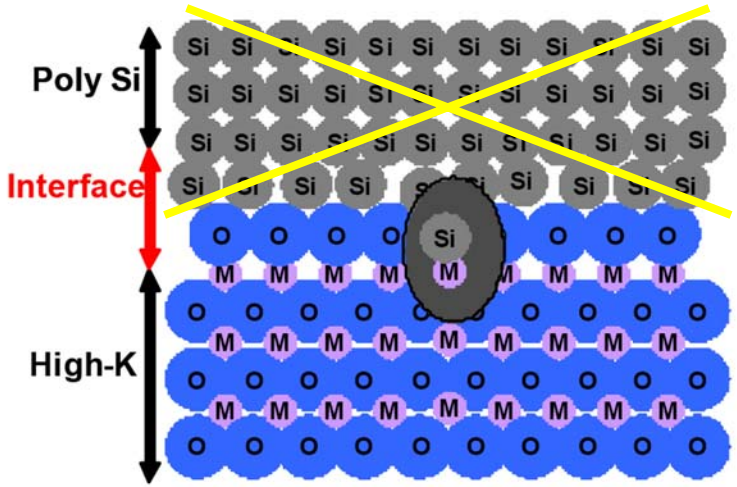


Fig. 4 Defect formation at the polySi and high-K dielectric interface is most likely the cause of the Fermi level pinning which causes high threshold voltages in MOSFET (M = Zr or Hf).

Replace poly Si with a metal gate whose work function minimizes Fermi level pinning

Different metals are required for NMOS and PMOS

R. Chan, "Advanced metal gate/high-k dielectric stacks for high-performance CMOS transistors," AVS 5th International Conference on Microelectronics and Interfaces, Santa Clara, California, March 1, 2004.

Limitations of CMOS at the Nanoscale

(3) Interconnects scale with channel length

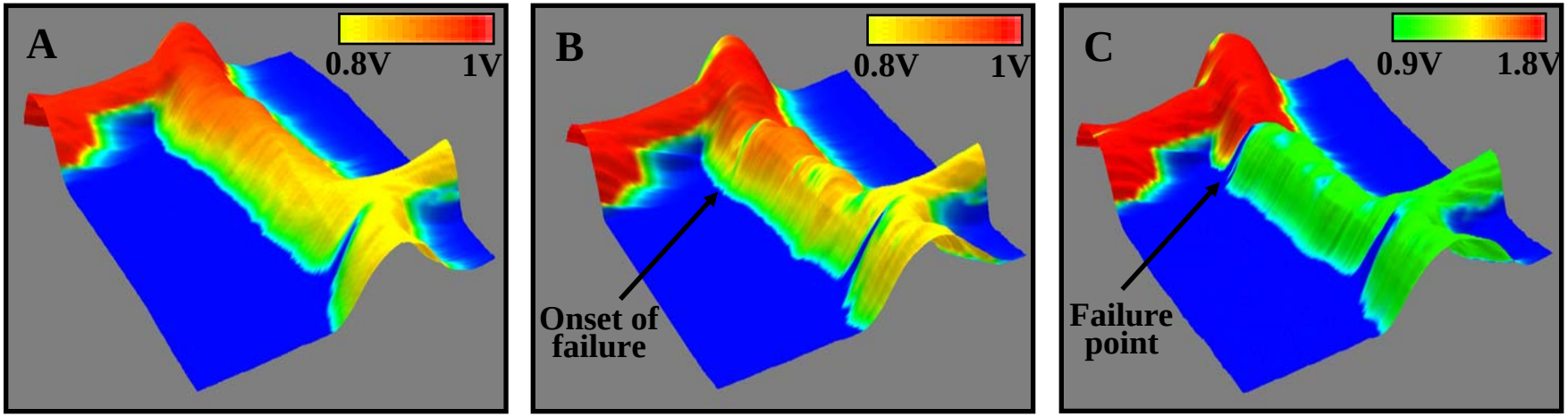
→ Higher $J = I/A$, $R = \rho l/A$

→ electromigration and other failure mechanisms

→ electromigration concerns motivated the switch from aluminum to copper interconnects

Potentiometry of Nanowire Failure

Evolution of nanowire failure:



Contact mode AFM potentiometry images: Wire width = 60 nm

(Breakdown current density = 3.75×10^{12} A/m^2).

M. C. Hersam, A. C. F. Hoole, S. J. O'Shea, and M. E. Welland, *Appl. Phys. Lett.*, 72, 915 (1998).

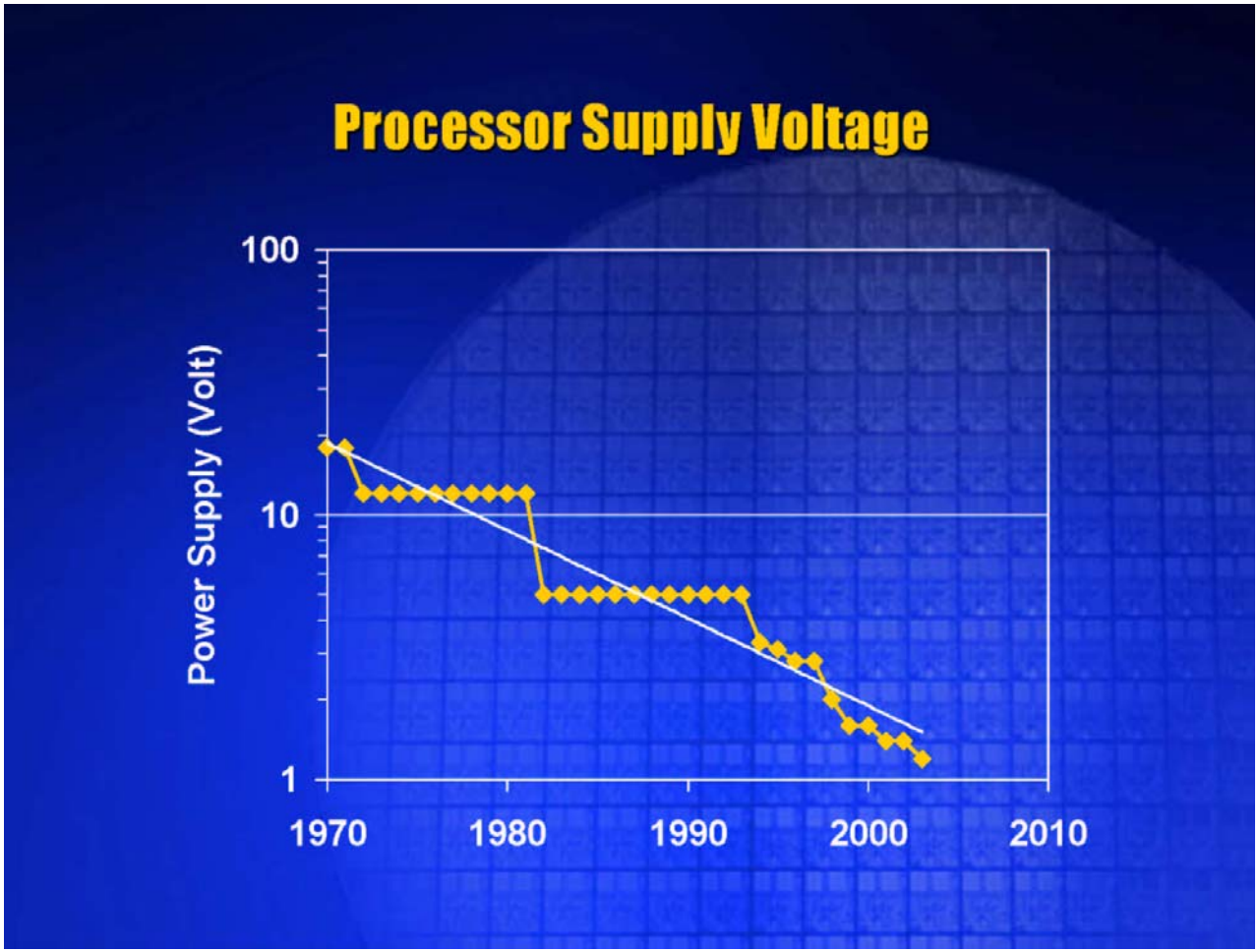
Limitations of CMOS at the Nanoscale

(4) Hot electron effects

→ As channel length decreases, E-field increases ($E = V/l$)

→ "Hot electrons" desorb hydrogen at interface
(replace with deuterium to increase lifetime)

→ Alternatively, decrease V → implies tighter control of noise and device characteristics



"No Exponential is Forever … but We Can Delay 'Forever',"
Gordon E. Moore, International Solid State Circuits Conference, Feb. 10, 2003.

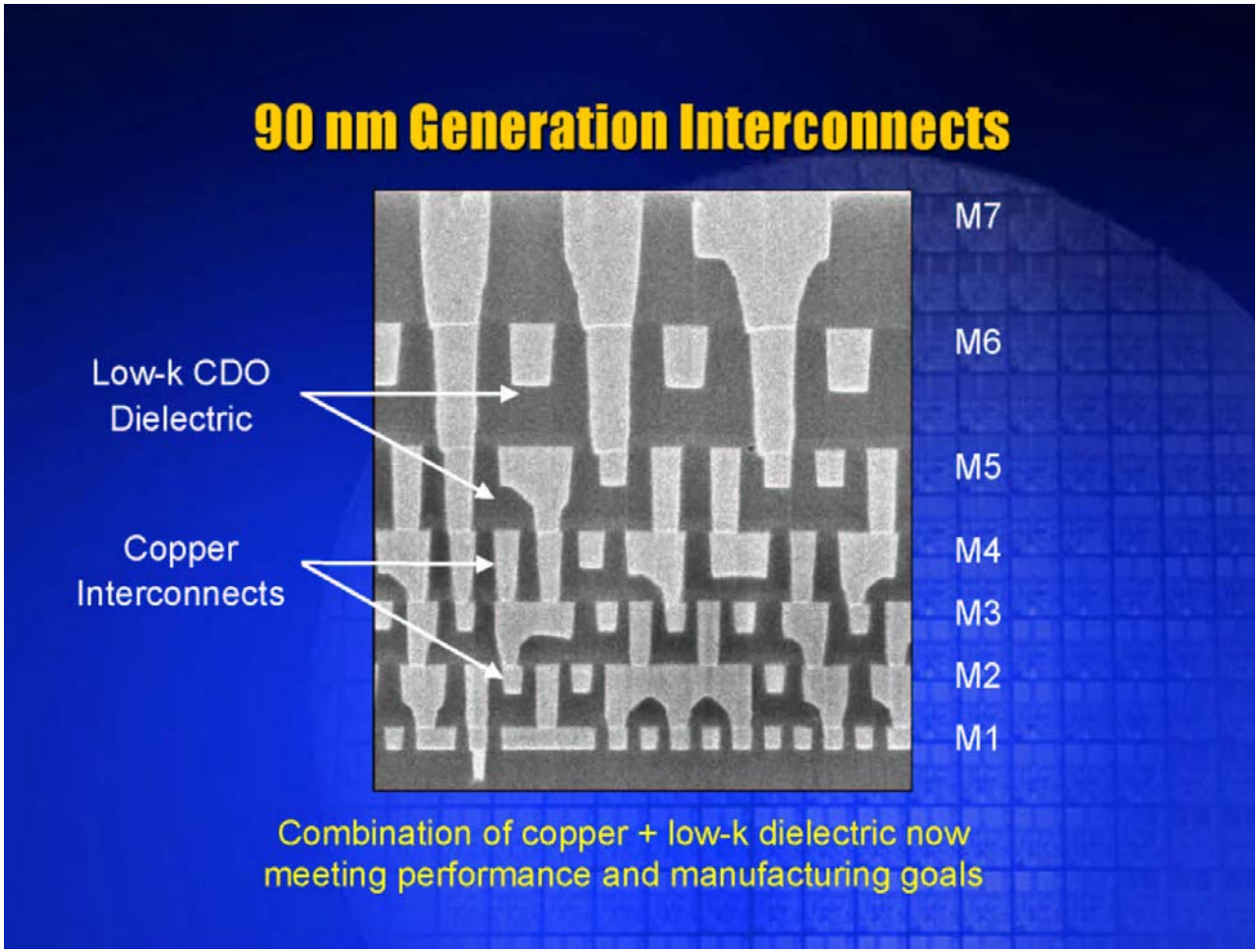
Limitations of CMOS at the Nanoscale

(5) Interconnect cross-talk

→ Capacitive coupling increases as spacing between interconnects decreases ($C = \varepsilon A/d$)

→ To decrease d, ε needs to be decreased

→ Low-k dielectric materials (porous materials)



"No Exponential is Forever … but We Can Delay 'Forever',"
Gordon E. Moore, International Solid State Circuits Conference, Feb. 10, 2003.

Limitations of CMOS at the Nanoscale

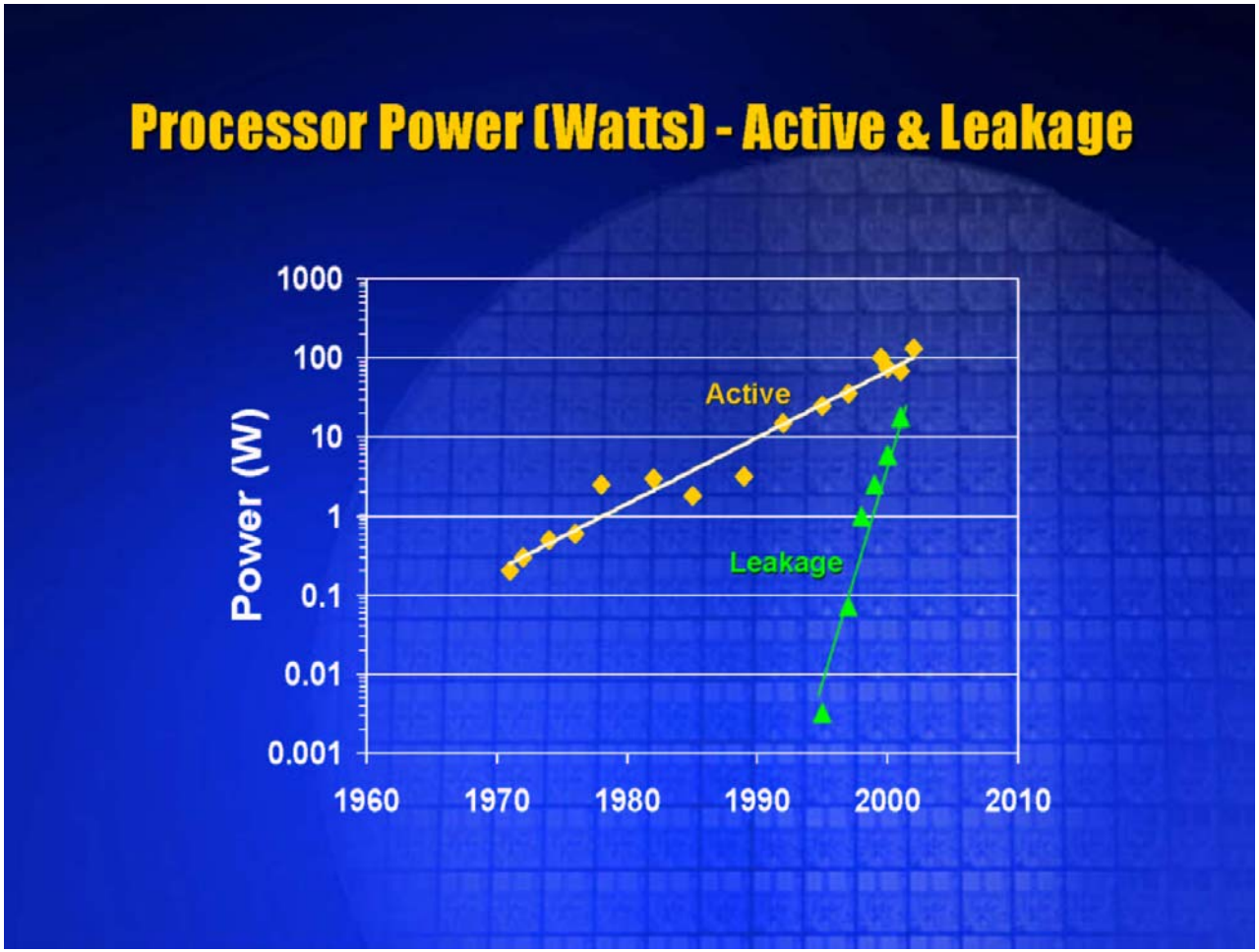
(6) Power Dissipation

→ Although CMOS ideally has no steady state power dissipation, power is dissipated during switching.

→ As clock speed and device densities increase, power dissipation increases

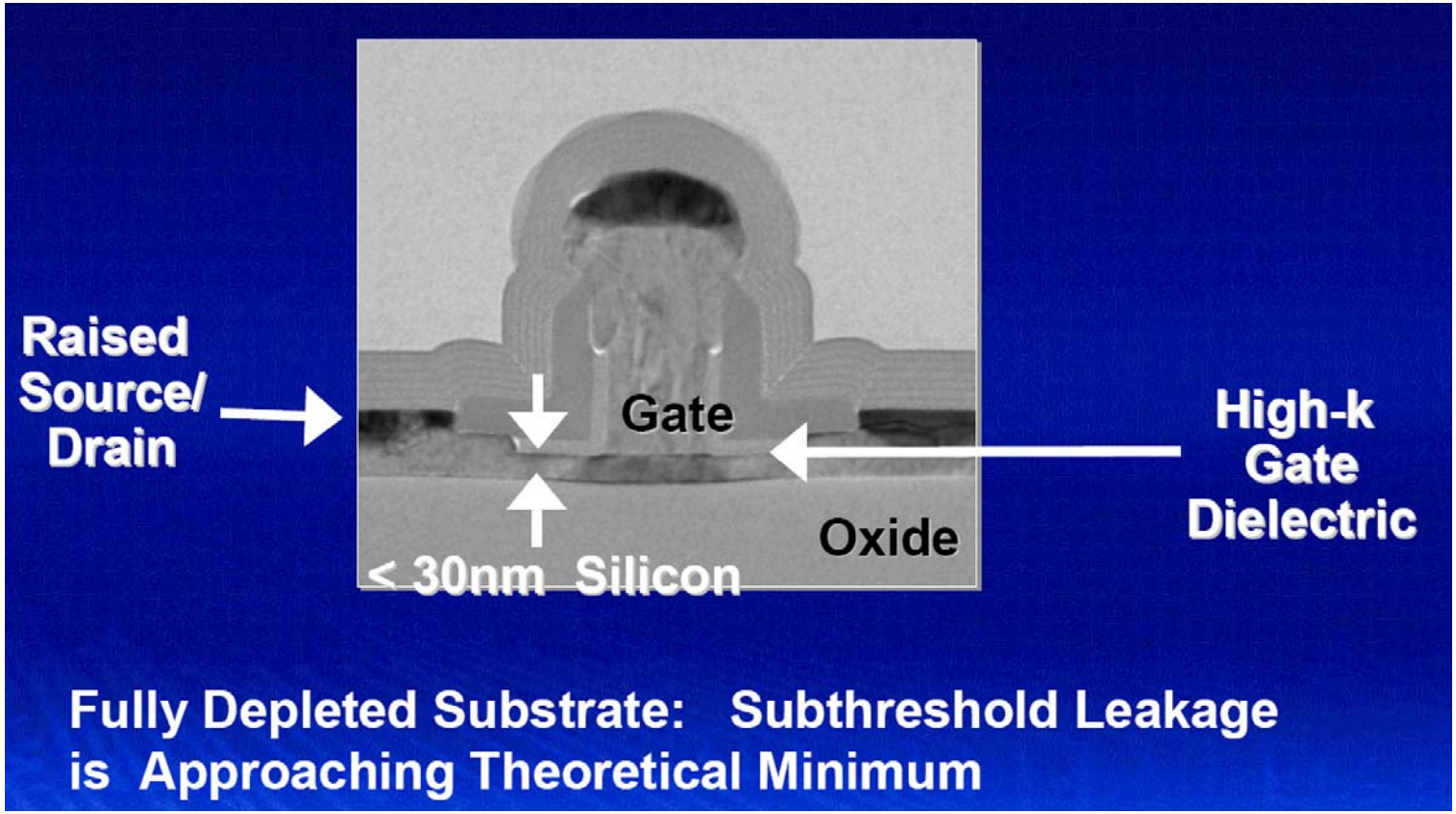
→ Steady state leakage power is also increasing due to gate leakage current and leakage to substrate

→ Gate leakage is minimized with high k dielectrics; substrate leakage is minimized with silicon-on-insulator



"No Exponential is Forever … but We Can Delay 'Forever',"
Gordon E. Moore, International Solid State Circuits Conference, Feb. 10, 2003.

Silicon-on-Insulator (SOI) Technology



G. Marcyk, "High performance non-planar tri-gate transistor architecture," Sept. 17, 2002.

Limitations of CMOS at the Nanoscale

(7) Operating speed

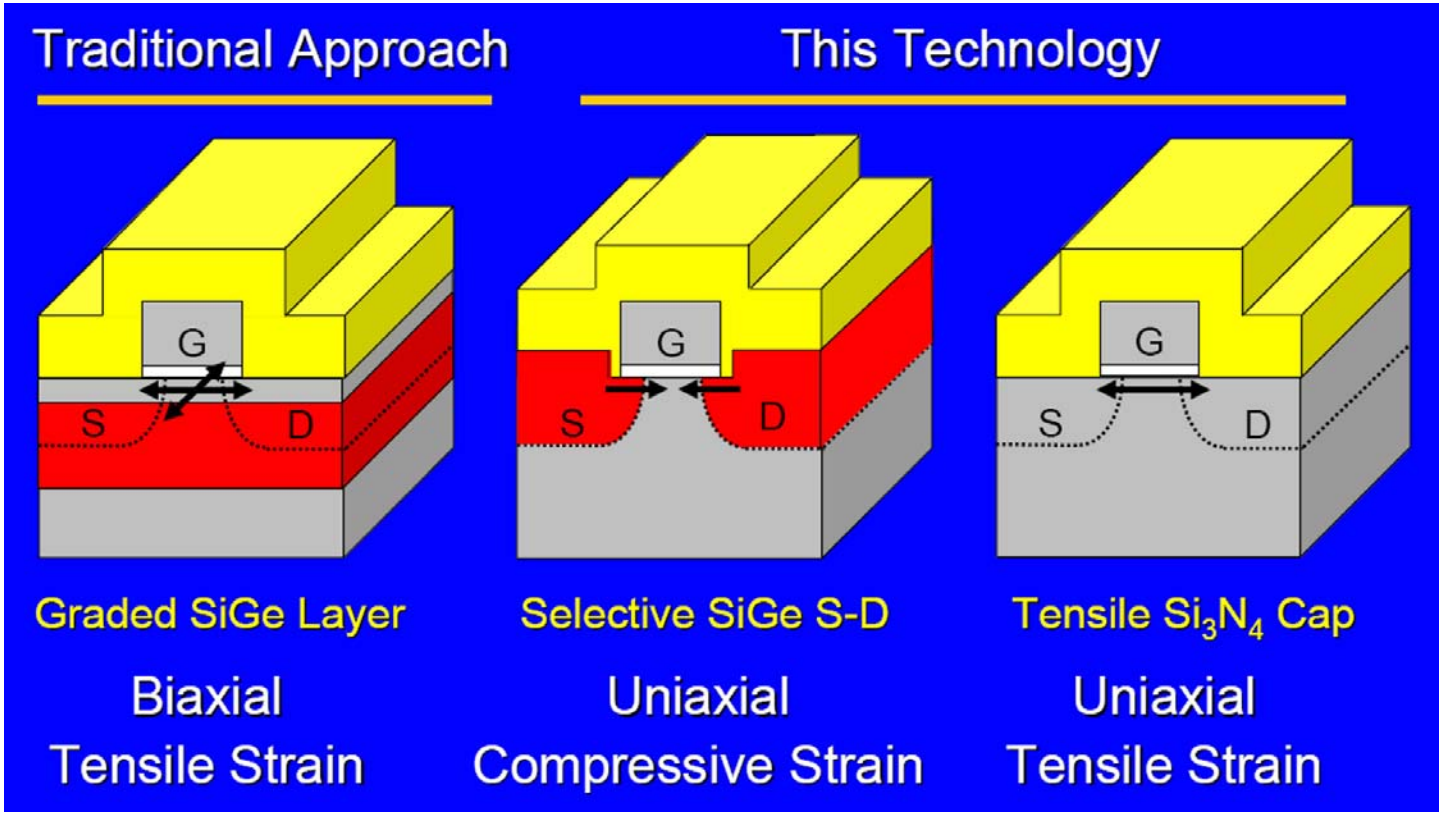
→ Speed is limited by charging time (i.e., *RC* time constant).

→ Low-k minimizes *C* and copper minimizes *R* for interconnects.

→ Transistor speed is limited by carrier mobility

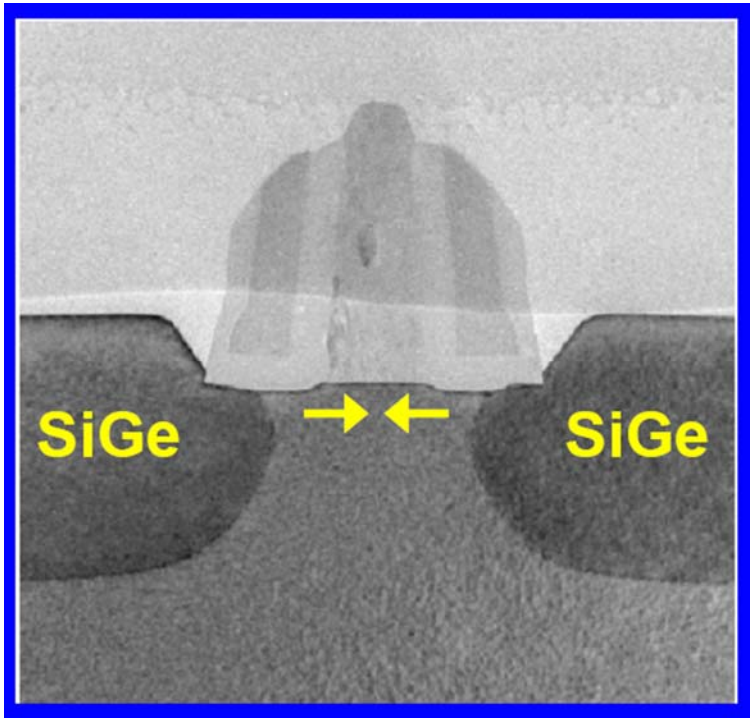
→ Carrier mobility is enhanced by intentionally introducing strain into the channel.

Transistor Strain Technologies



T. Ghani, et al., "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," International Electron Devices Meeting, December 9, 2003.

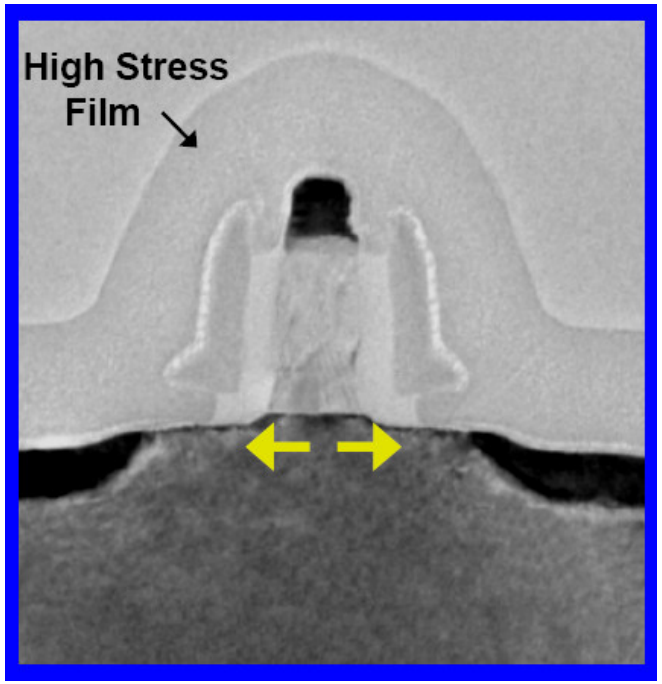
PMOS Strain Technology: Enhancing Hole Mobility Through Uniaxial Compressive Strain



Embedded geometry +
compressive source/drain =
Large uniaxial compressive strain

T. Ghani, et al., "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," International Electron Devices Meeting, December 9, 2003.

NMOS Strain Technology: Enhancing Electron Mobility Through Uniaxial Tensile Strain



Highly tensile silicon nitride capping film

T. Ghani, et al., "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," International Electron Devices Meeting, December 9, 2003.

Limitations of CMOS at the Nanoscale

(8) Cost

→ Revenues increase by ~16%/year

→ Factory cost increases by ~19%/year

→ Plus, advanced lithographies (e-beam, ion beam, X-ray, EUV) are currently more expensive than DUV lithography

→ Costs are expected to rise more quickly than revenues in the future

"Moore's Law" for CMOS Economics

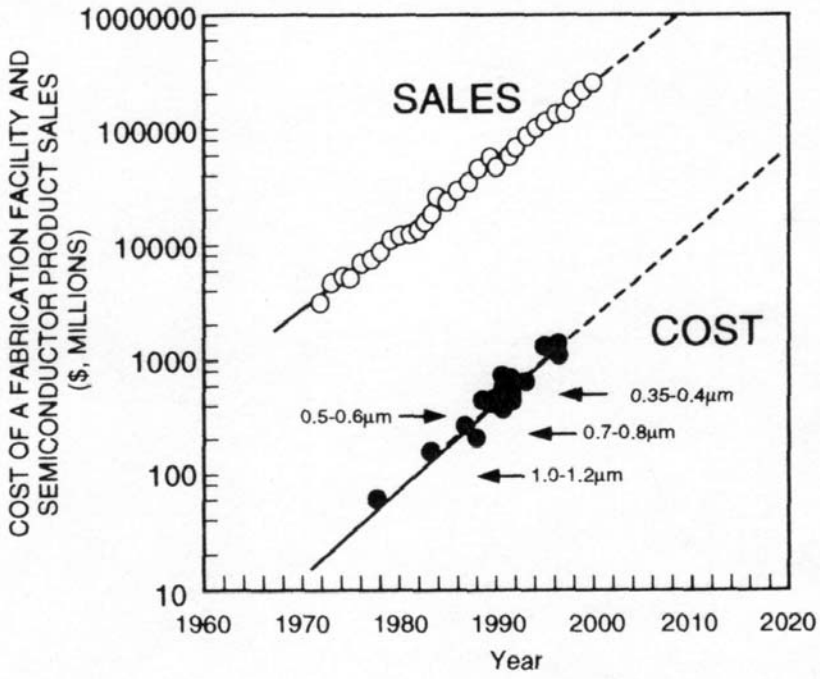
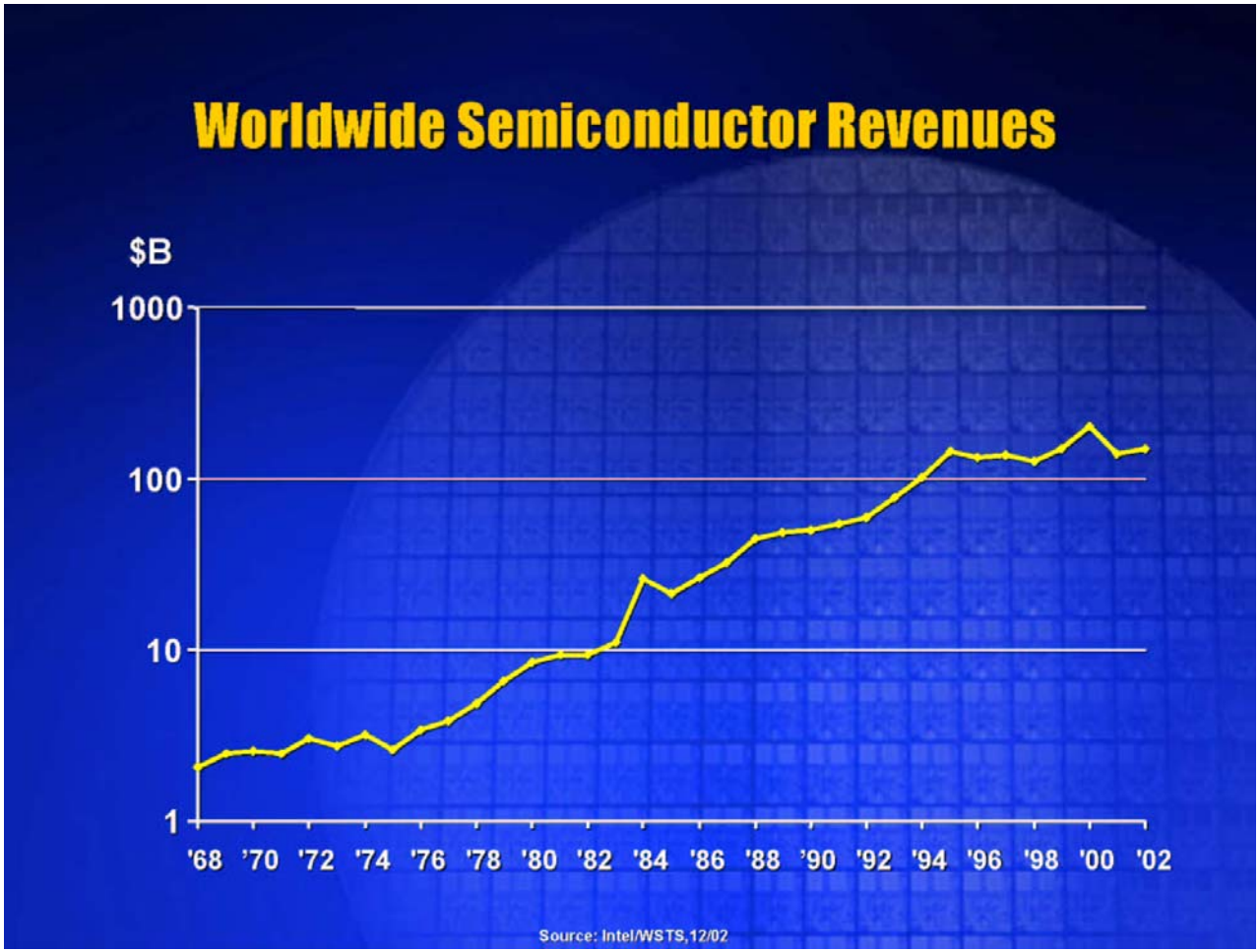
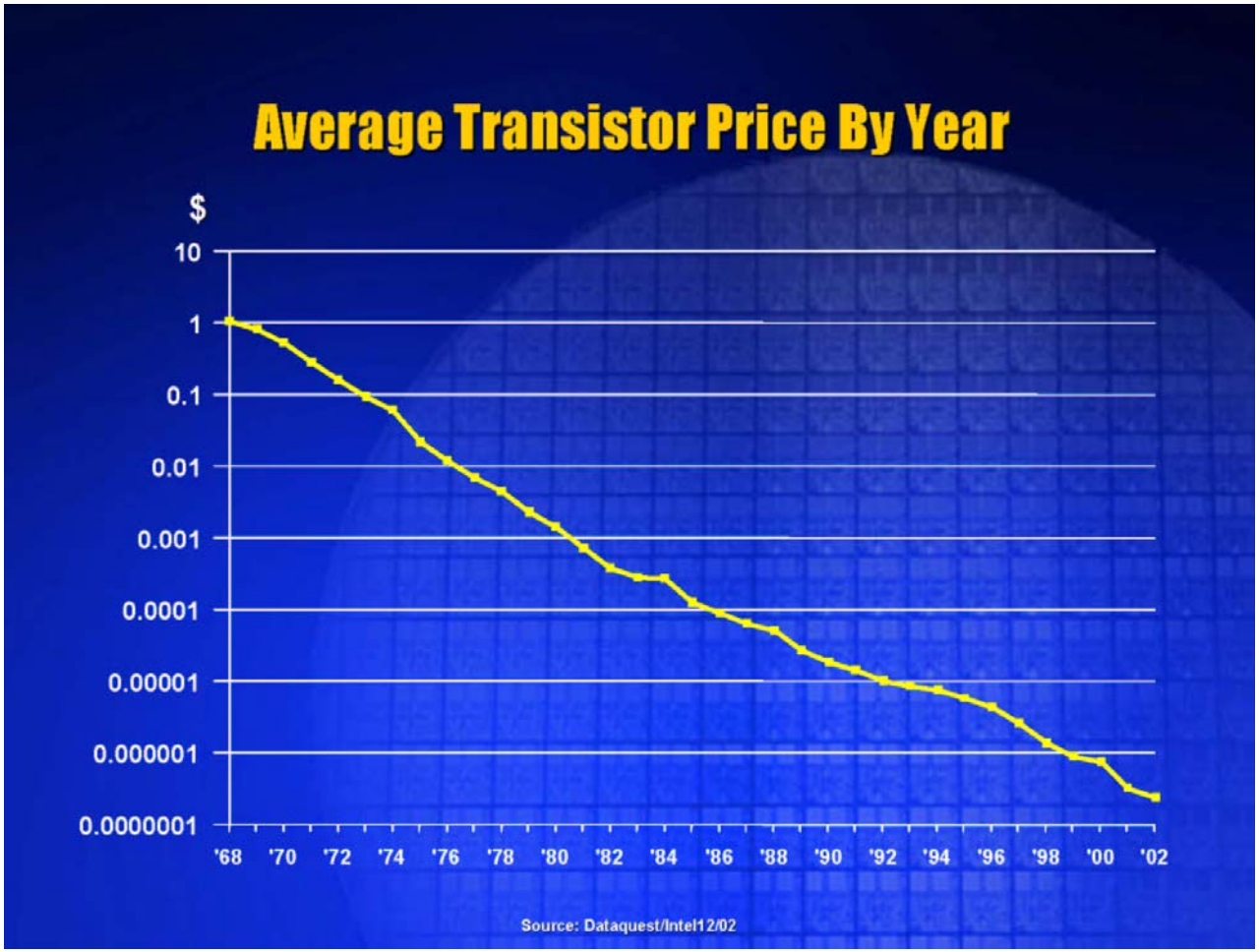


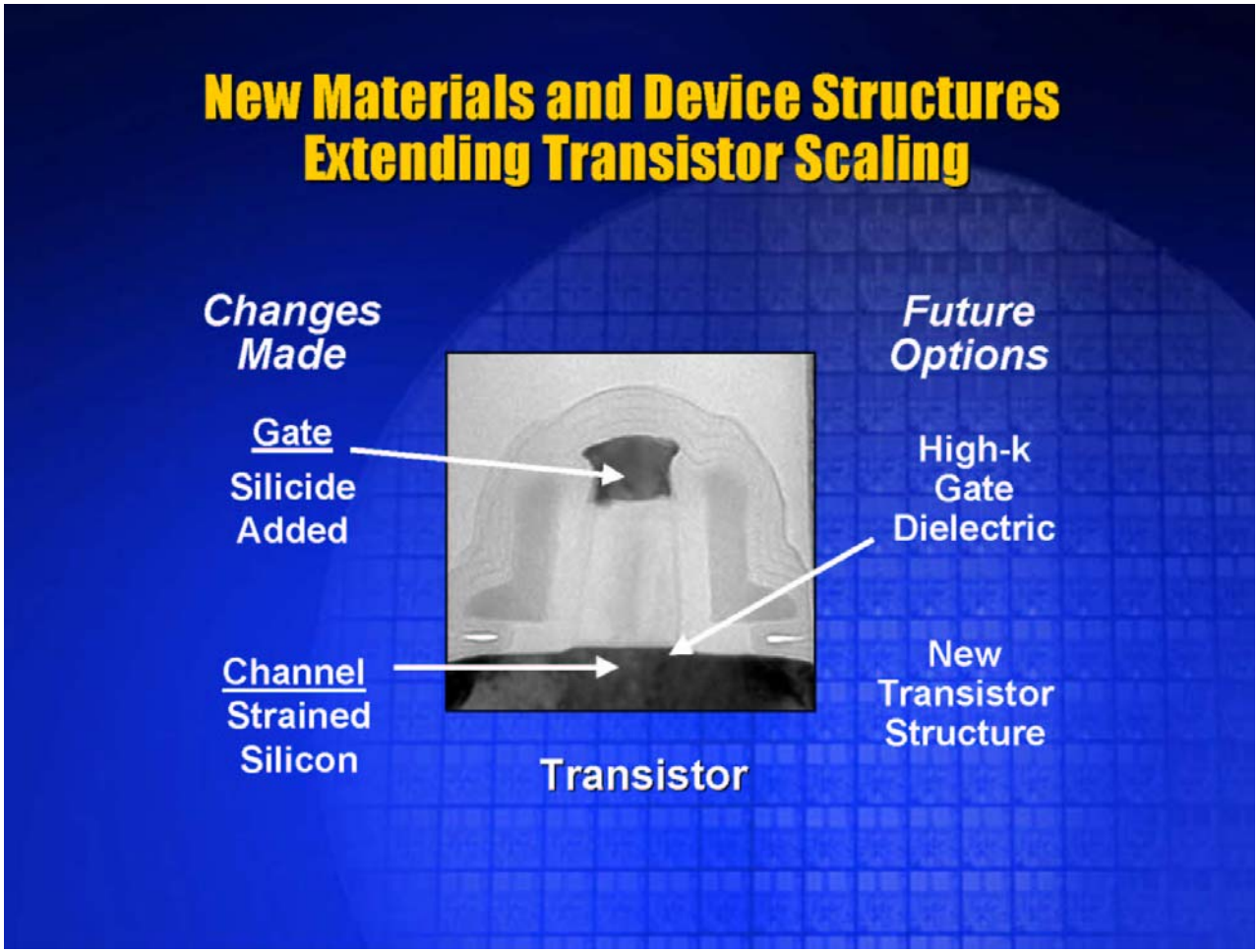
FIGURE 3. A compilation of estimates of the required capital investment for a large semiconductor fabrication line taken from the SEMATECH[165] and the estimated world-wide semiconductor electronics (IC) sales taken from DataQuest, Makimoto[10] and Bois[11]. The year for introduction of a particular technology, denoted by the design rule, e.g. 0.35 μm, is plotted versus millions of U.S. dollars.



"No Exponential is Forever … but We Can Delay 'Forever',"
Gordon E. Moore, International Solid State Circuits Conference, Feb. 10, 2003.



"No Exponential is Forever … but We Can Delay 'Forever',"
Gordon E. Moore, International Solid State Circuits Conference, Feb. 10, 2003.



"No Exponential is Forever … but We Can Delay 'Forever',"
Gordon E. Moore, International Solid State Circuits Conference, Feb. 10, 2003.

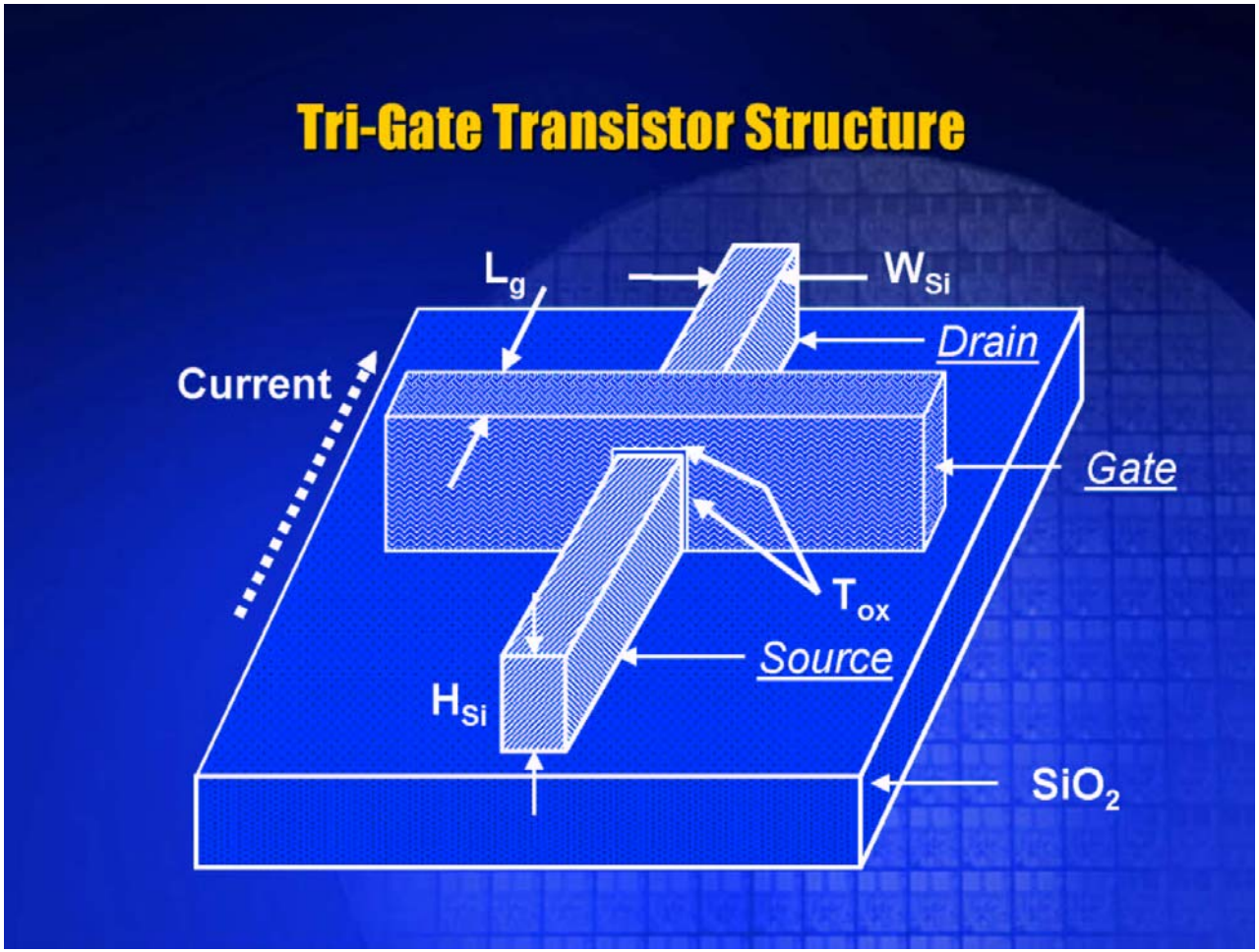
Start Dates for New Materials

Process Name	P856	P858	Px60	P1262	P1264	P1266	P1268	P1270
1st Production	1997	1999	2001	2003	2005	2007	2009	2011
Process Generation	0.25μm	0.18μm	0.13μm	90 nm	65 nm	45 nm	32 nm	22 nm
Wafer Size (mm)	200	200	200/300	300	300	300	300	300
Inter-connect	Al	Al	Cu	Cu	Cu	Cu	Cu	?
Channel	Si	Si	Si	Strained Si	Strained Si	Strained Si	Strained Si	Strained Si
Gate dielectric	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	High-k	High-k	High-k
Gate electrode	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Metal	Metal	Metal

Introduction targeted at this time

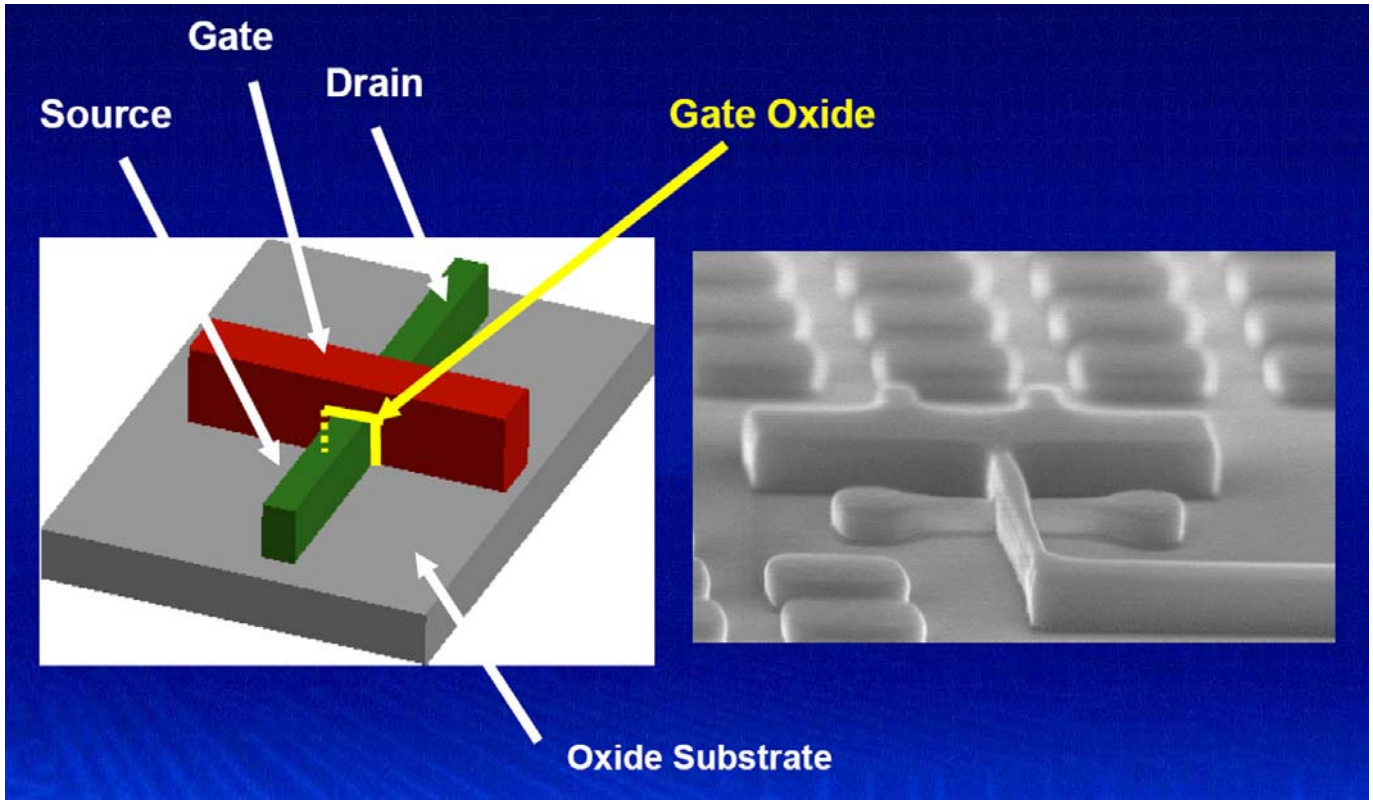
Subject to change

"Intel's High-k/Metal Gate Announcement," November 5, 2003.



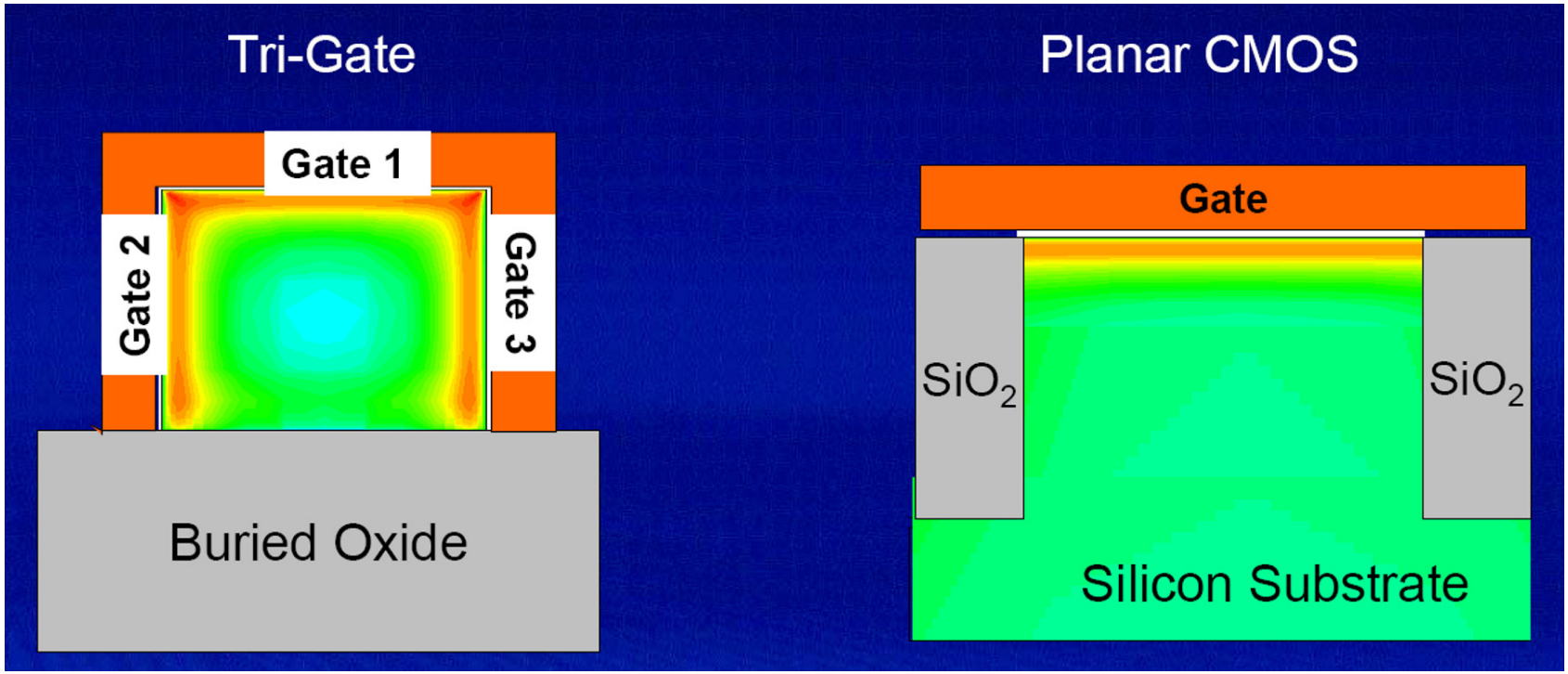
"No Exponential is Forever … but We Can Delay 'Forever',"
Gordon E. Moore, International Solid State Circuits Conference, Feb. 10, 2003.

Fabricated Tri-Gate Transistor



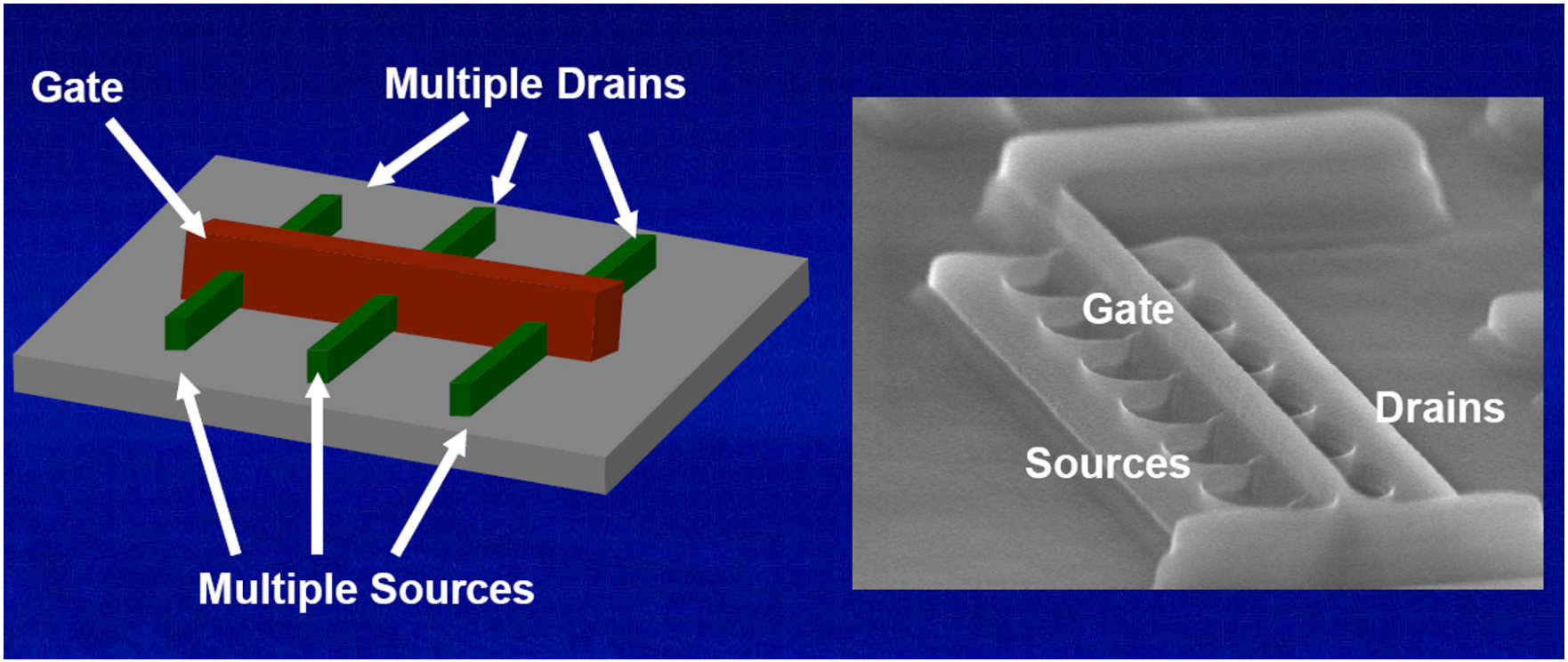
G. Marcyk, "High performance non-planar tri-gate transistor architecture," Sept. 17, 2002.

Complete Depletion of Tri-Gate Transistor

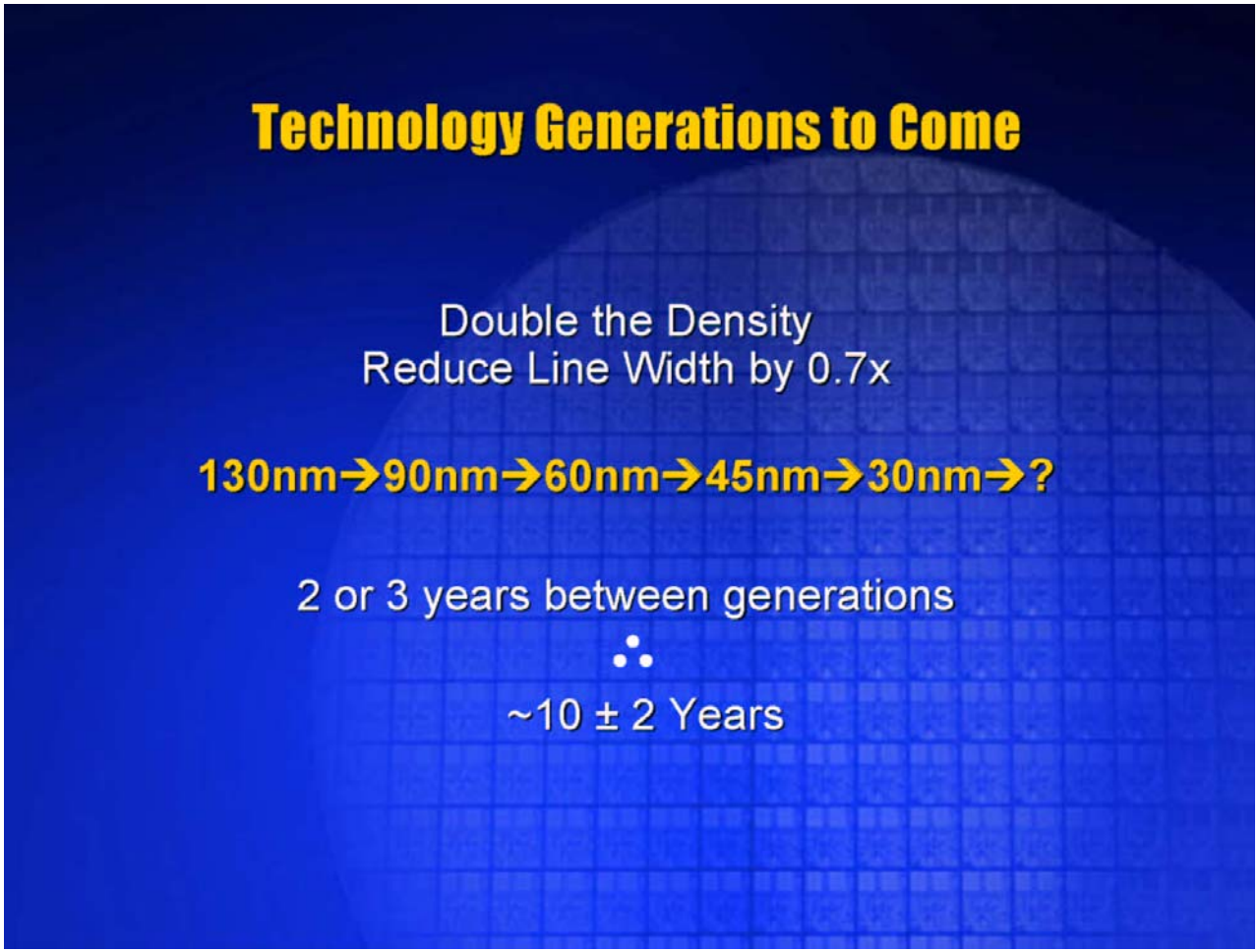


G. Marcyk, "High performance non-planar tri-gate transistor architecture," Sept. 17, 2002.

Multi-Channel Tri-Gate Transistors Enable More Drive Current

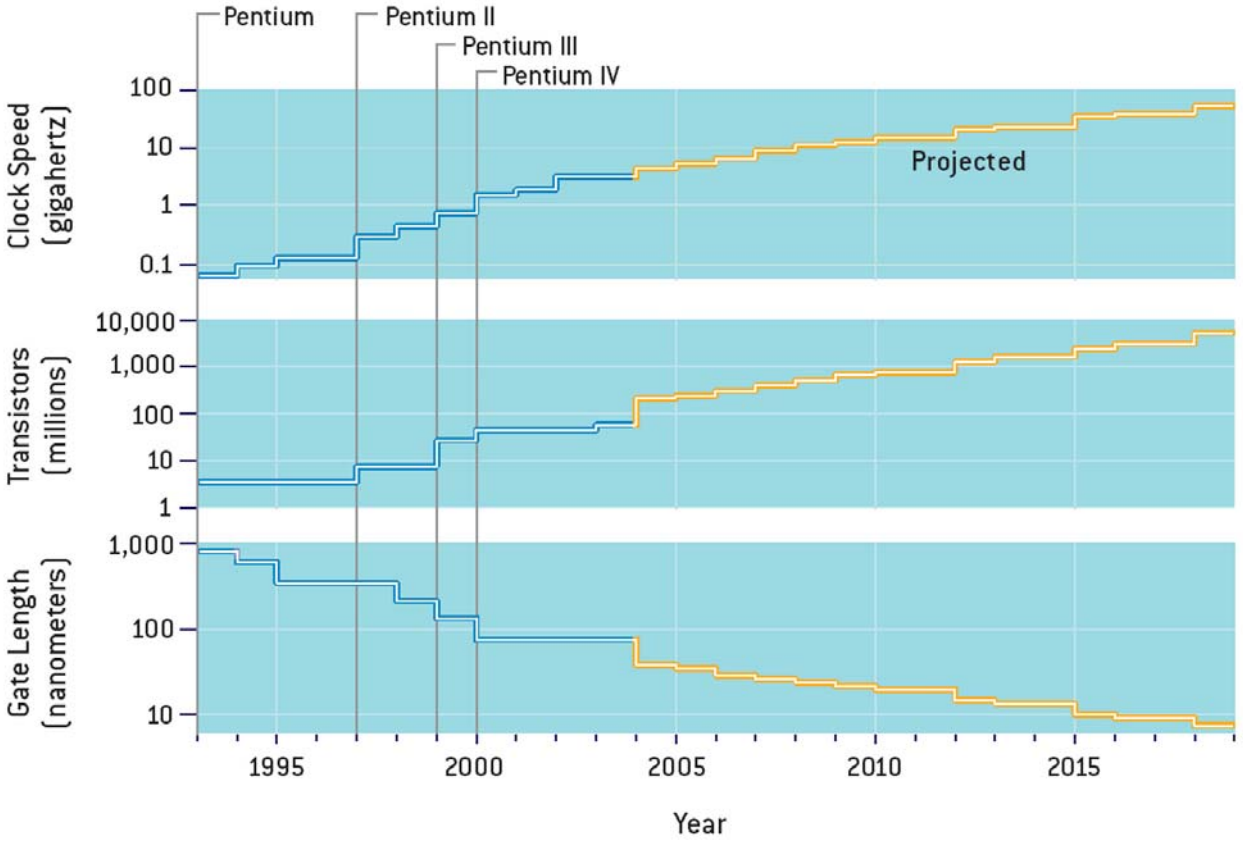


G. Marcyk, "High performance non-planar tri-gate transistor architecture," Sept. 17, 2002.



"No Exponential is Forever … but We Can Delay 'Forever',"
Gordon E. Moore, International Solid State Circuits Conference, Feb. 10, 2003.

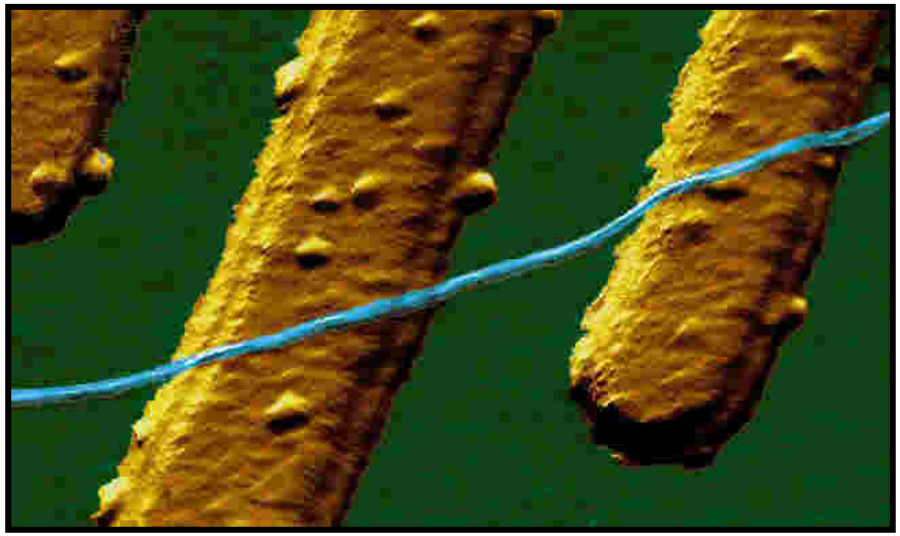
Semiconductor Industry Roadmap



G. D. Hutcheson, *Scientific American*, April, 2004, p. 76.

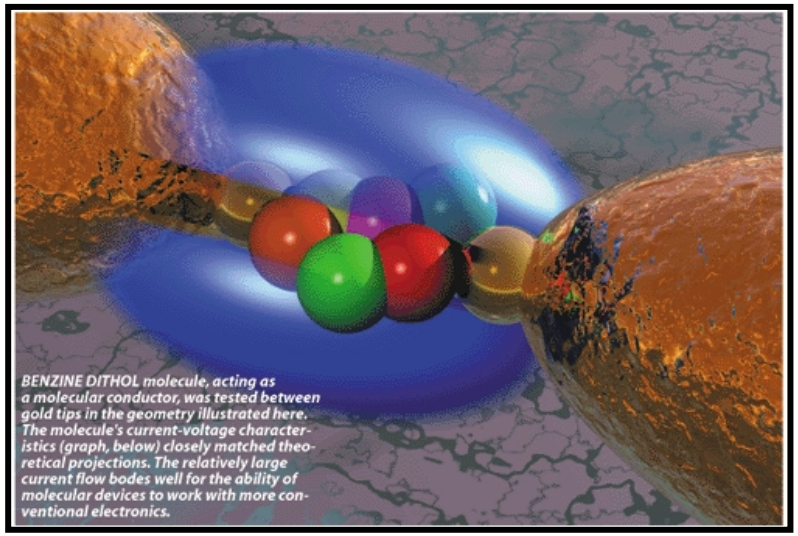
Nanoelectronic Alternatives

Carbon Nanotube Transistors



Nature, **391**, 59 (1998).

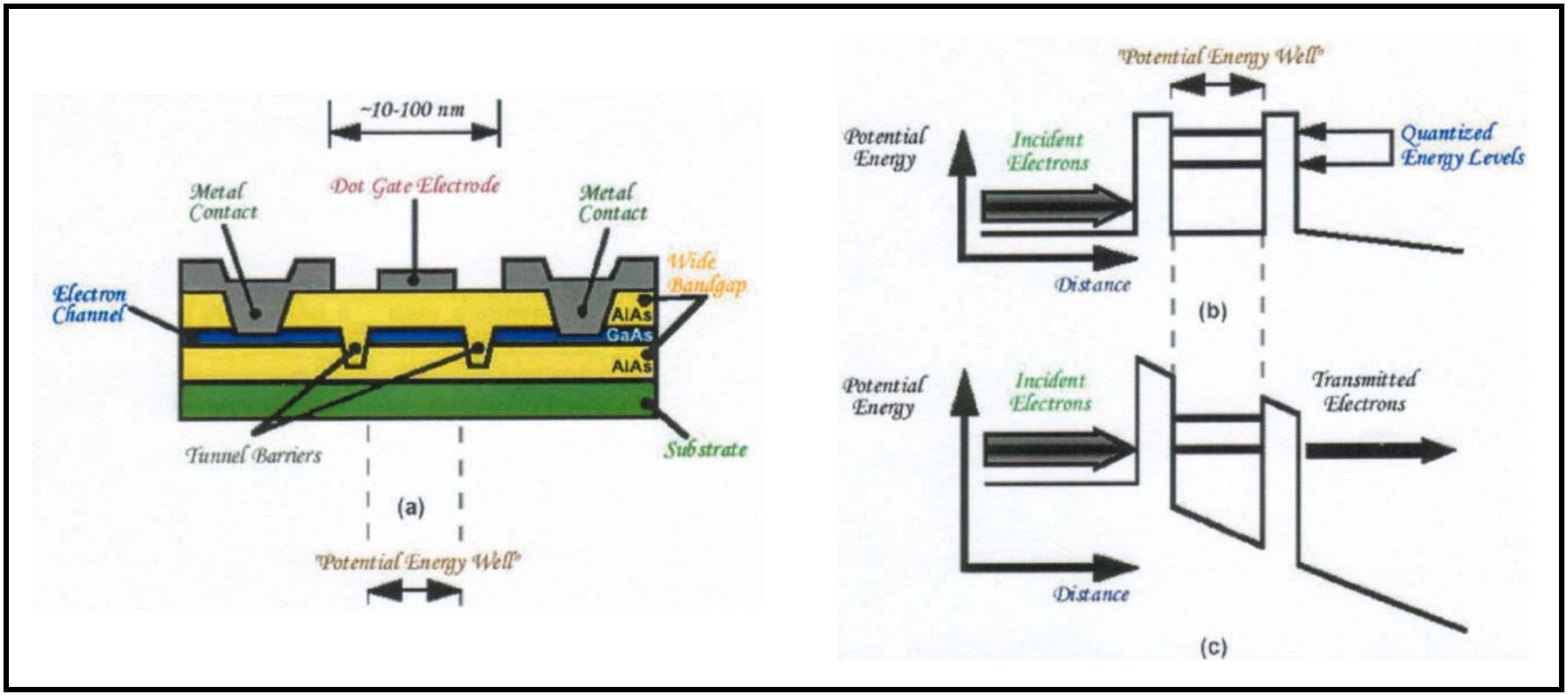
Molecular Electronics



Sci. American, **282**, 86 (2000).

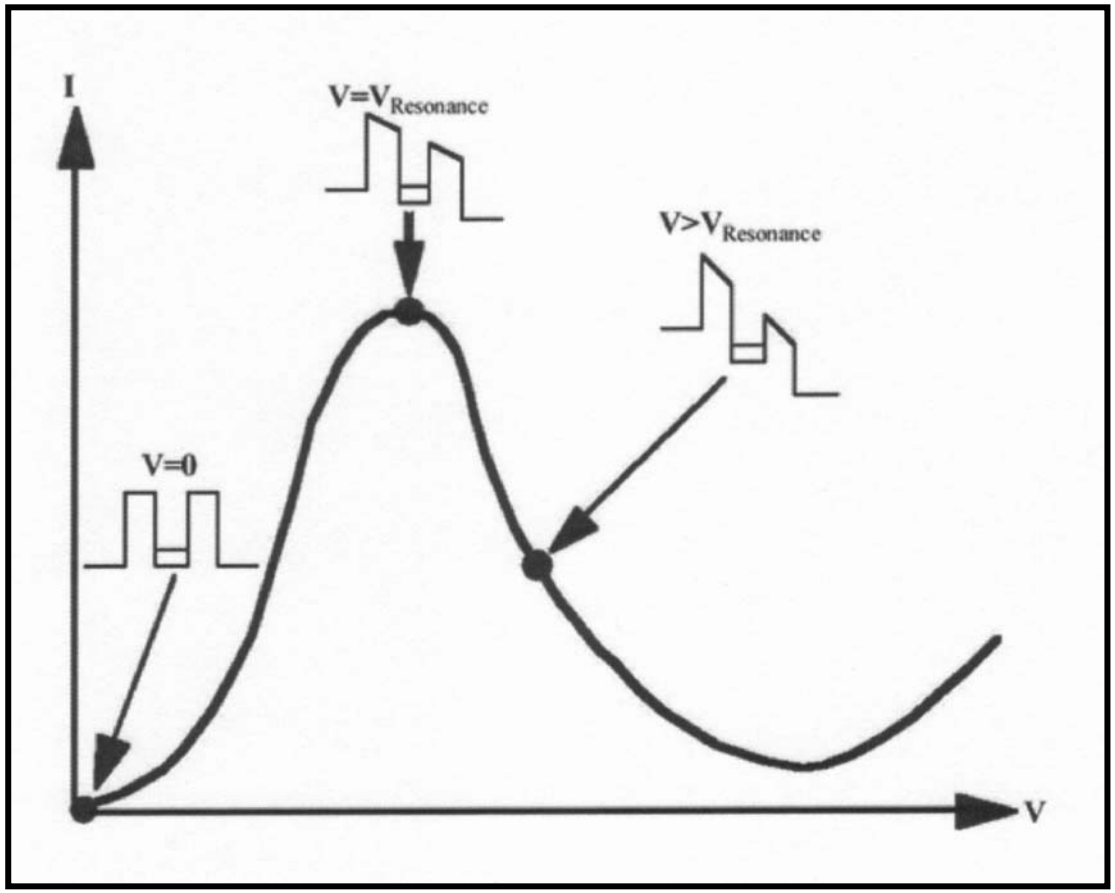
Resonant Tunneling Diodes, Single Electron Devices, Quantum Cellular Automata, Molecular Electronics, …

Resonant Tunneling Diode



http://courses.nus.edu.sg/course/phyweets/Projects99/Quantum

Negative Differential Resistance



http://courses.nus.edu.sg/course/phyweets/Projects99/Quantum

Single Electron Devices

Coulomb Blockade: Suppression of electron tunneling to an island (0-D quantum dot) by a single electron charging energy

NOTE: Capacitor charging energy = $Q^2/2C$
For a single electron → $e^2/2C$

Two Conditions for Coulomb Blockade:

(1) Thermal Fluctuations: $e^2/C >> kT$

(2) Heisenberg Uncertainty: $\Delta E \Delta t >> h$
$(e^2/C)(R_tC) >> h \rightarrow R_t >> h/e^2$

Temperature Requirement for Coulomb Blockade

Temperature Condition for Coulomb Blockade:

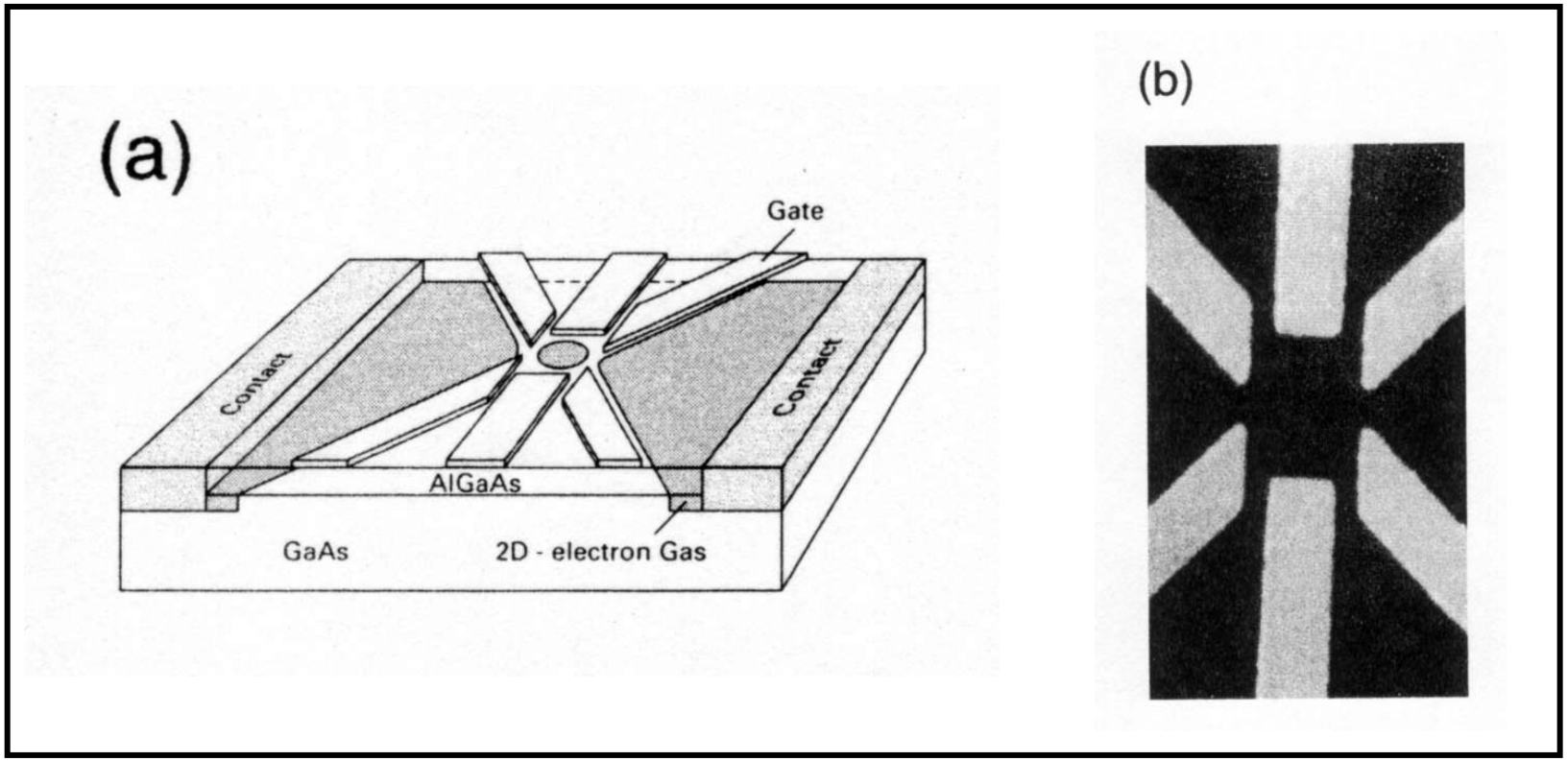
To suppress thermal fluctuations, $e^2/C >> kT$

→ For room temperature operation, C ~ 1 aF = 10^{-18} F

→ For C ~ 1 aF, quantum dot dimensions ~ 1 nm

→ Since it is challenging to fabricate down to 1 nm, most single electron devices only operate at low temperature

GaAs/AlGaAs Single Electron Device



Top gates deplete 2-DEG, thus forming a quantum dot

Coulomb Blockade I-V Characteristic

Single Electron Transistor

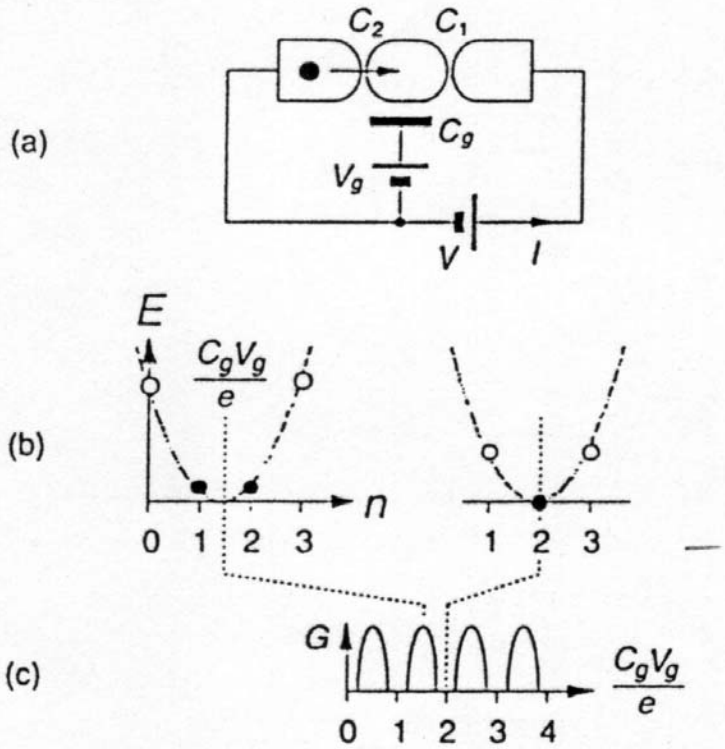


Fig. 2. Operating principle of a single electron transistor. (a) Configuration. (b) Charging energy as a function of the number of excess electrons on the central island. (c) Conductance as a function of gate voltage.

Single Electron Transistor

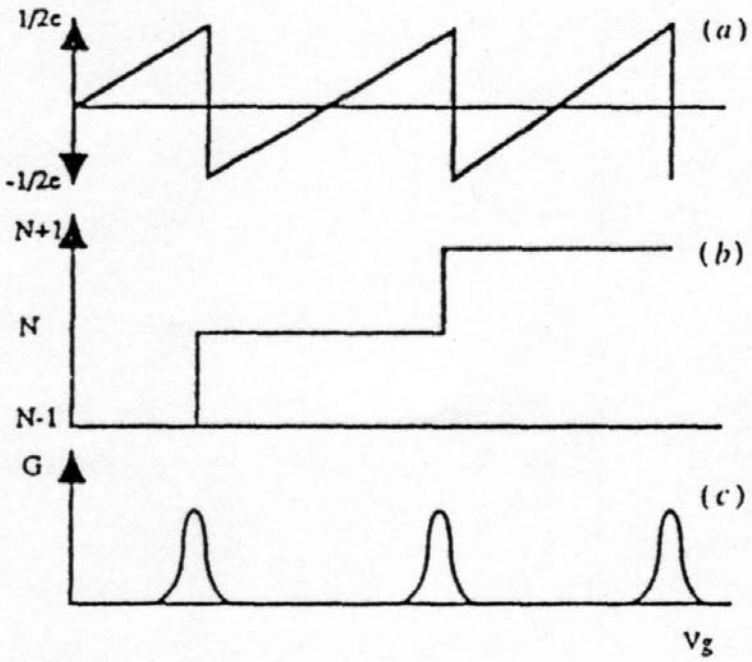


Fig. 3. A plot of: (a) charge; (b) number of electrons; and (c) conductance through a dot versus gate voltage.

Single Electronics

Benefits:

(1) Low power since only one electron moves through the device

(2) High device density is possible

Problems:

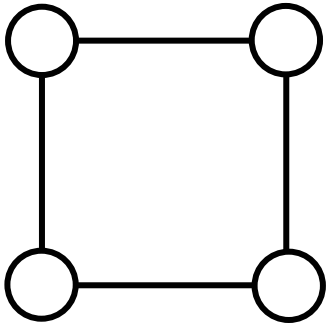
(1) Fabrication is difficult

(2) Inherently slow since only one electron moves through the device
→ Difficult to charge up capacitance at outputs (fan-out problems)

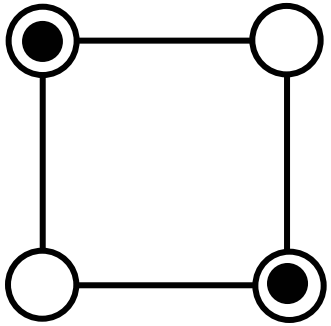
(3) Interconnections

Quantum Cellular Automata

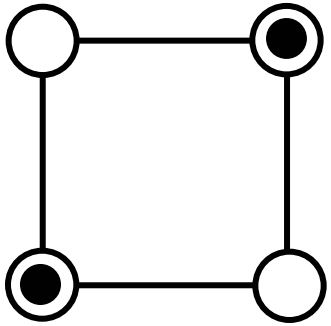
Consider four coupled quantum dots:



If two electrons are injected into this cell, there are two possibilities that minimize electrostatic energy:



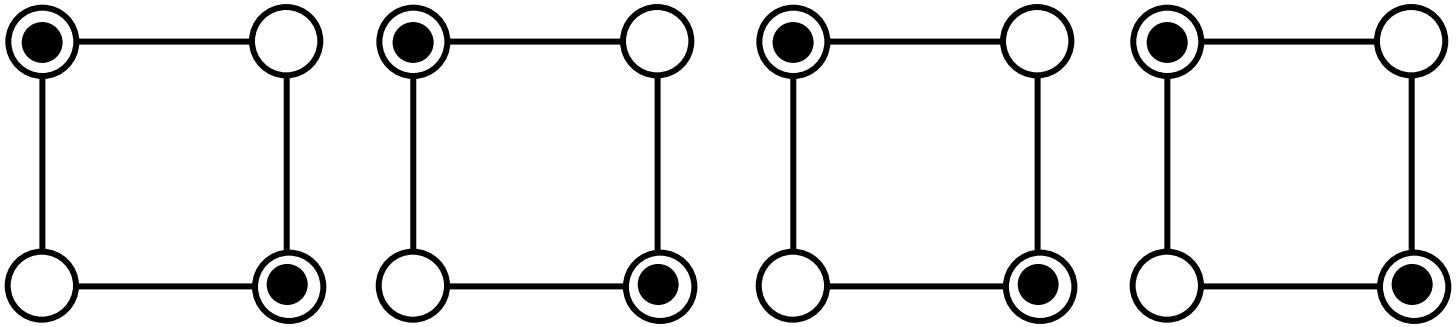
OR



“0” **“1”**

Quantum Cellular Automata

Adjacent QCA cells align to minimize electrostatic energy:



- If you switch the first cell, the other cells will follow

→ Information transfer without electron transfer
→ No interconnections are required between cells

- Intersecting QCA rows allow for logic and computation

Quantum Cellular Automata

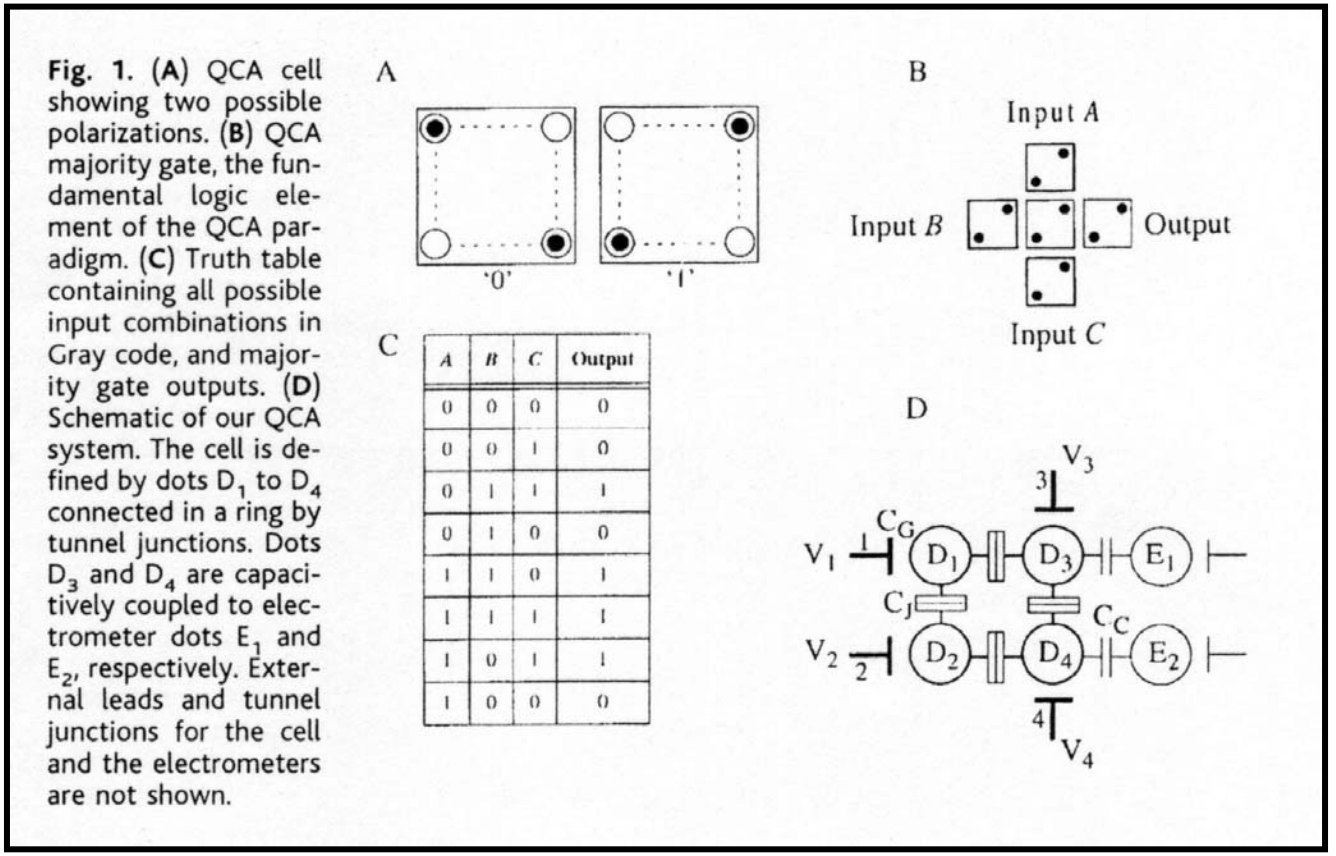


Fig. 1. (**A**) QCA cell showing two possible polarizations. (**B**) QCA majority gate, the fundamental logic element of the QCA paradigm. (**C**) Truth table containing all possible input combinations in Gray code, and majority gate outputs. (**D**) Schematic of our QCA system. The cell is defined by dots D_1 to D_4 connected in a ring by tunnel junctions. Dots D_3 and D_4 are capacitively coupled to electrometer dots E_1 and E_2, respectively. External leads and tunnel junctions for the cell and the electrometers are not shown.

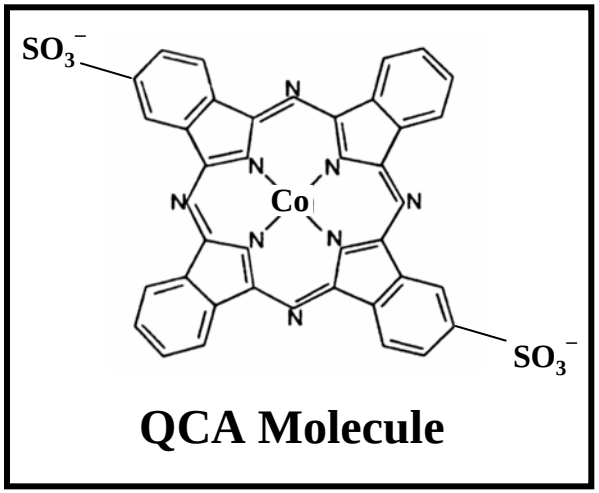
A	B	C	Output
0	0	0	0
0	0	1	0
0	1	1	1
0	1	0	0
1	1	0	1
1	1	1	1
1	0	1	1
1	0	0	0

I. Amlani, *et al.*, *Science*, **284**, 289 (1999).

Quantum Cellular Automata

• Although QCA minimizes the number of interconnections, it still suffers from the same thermal fluctuation problems as single electronic devices

• Consequently, QCA must be implemented at low temperatures or at molecular length scales:

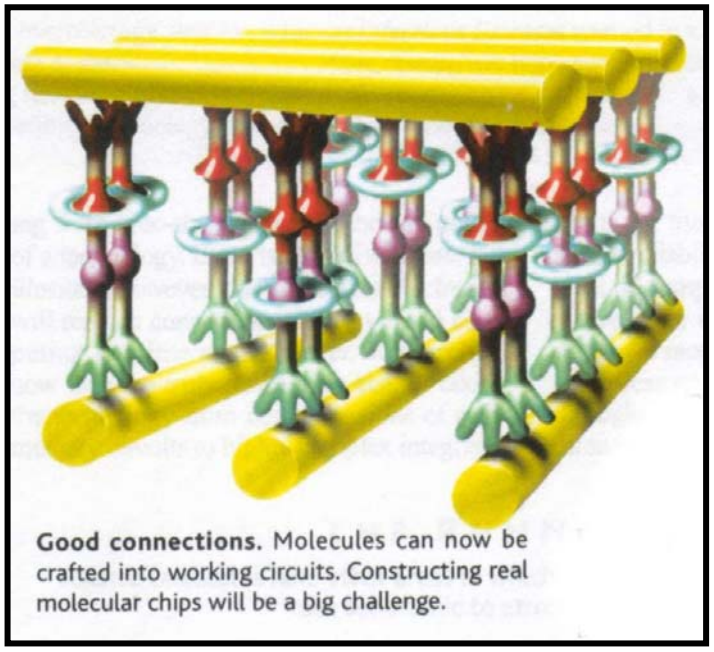


QCA Molecule

BREAKTHROUGH OF THE YEAR

In 2001, scientists assembled molecules into basic circuits, raising hopes for a new world of nanoelectronics

Molecules Get Wired



Good connections. Molecules can now be crafted into working circuits. Constructing real molecular chips will be a big challenge.

Science, **294**, 2442 (2001).

Contacting Molecules with Break Junctions

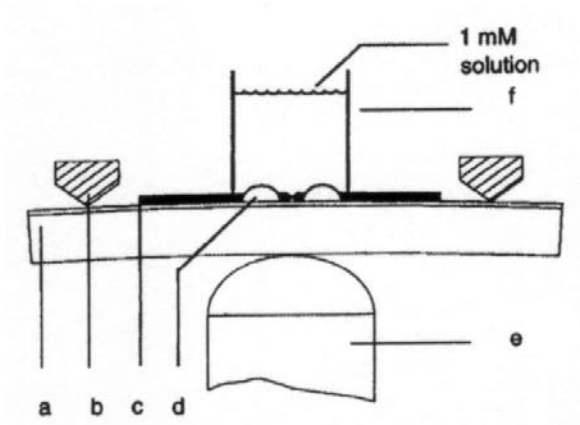


Fig. 1. A schematic of the MCB junction with (a) the bending beam, (b) the counter supports, (c) the notched gold wire, (d) the glue contacts, (e) the pizeo element, and (f) the glass tube containing the solution.

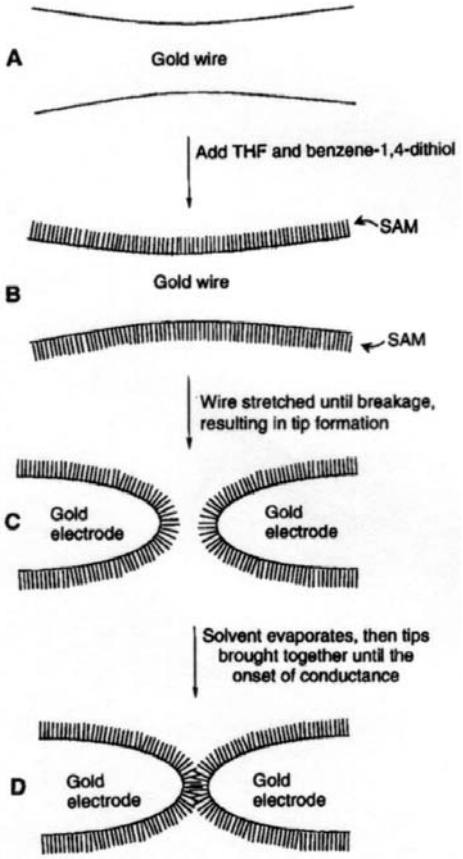


Fig. 2. Schematic of the measurement process. (**A**) The gold wire of the break junction before breaking and tip formation. (**B**) After addition of benzene-1,4-dithiol, SAMs form on the gold wire surfaces. (**C**) Mechanical breakage of the wire in solution produces two opposing gold contacts that are SAM-covered. (**D**) After the solvent is evaporated, the gold contacts are slowly moved together until the onset of conductance is achieved. Steps (C) and (D) (without solution) can be repeated numerous times to test for reprodicibility.

M. A. Reed, *et al.*, *Science*, **278**, 252 (1997).

Room Temperature Molecular Conduction

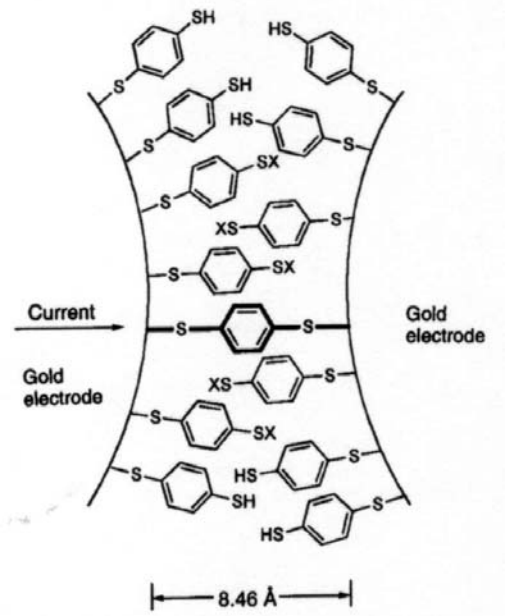


Fig. 3. A schematic of a benzene-1,4-dithiolate SAM between proximal gold electrodes formed in an MCB. The thiolate is normally H-terminated after deposition; end groups denoted as X can be either H or Au, with the Au potentially arising from a previous contact/retraction event. These molecules remain nearly perpendicular to the Au surface, making other molecular orientations unlikely (*21*).

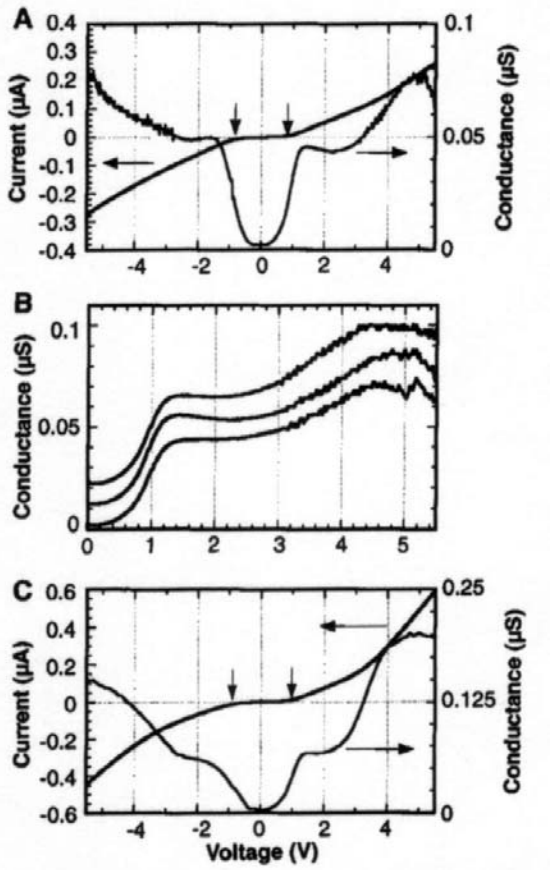


Fig. 4. (**A**) Typical *I*(*V*) characteristics, which illustrate a gap of 0.7 V; and the first derivative *G*(*V*), which shows a steplike structure. (**B**) Three independent *G*(*V*) measurements, offset for clarity, illustrating the reproducibility of the conductance values. The measurements were made with the same MCB but for different retractions/contacts and thus different contact configurations. Offsets of 0.01 μS for the middle curve and 0.02 μS for the top curve are used for clarity. The first step for these three measurements gives values of 22.2, 22.2, and 22.7 megohm (top to bottom); the next step gives values of 12.5, 13.3, and 14.3 megohm. The middle curve is the same data as in (A). (**C**) An *I*(*V*) and *G*(*V*) measurement illustrating conductance values approximately twice the observed minimum conductance values. Resistances of ~14 megohm for the first step and 7.1 megohm (negative bias) and 5 megohm (positive bias) for the second step were measured.

M. A. Reed, *et al.*, *Science*, **278**, 252 (1997).

Contacting Molecules with Nanoscale Pores

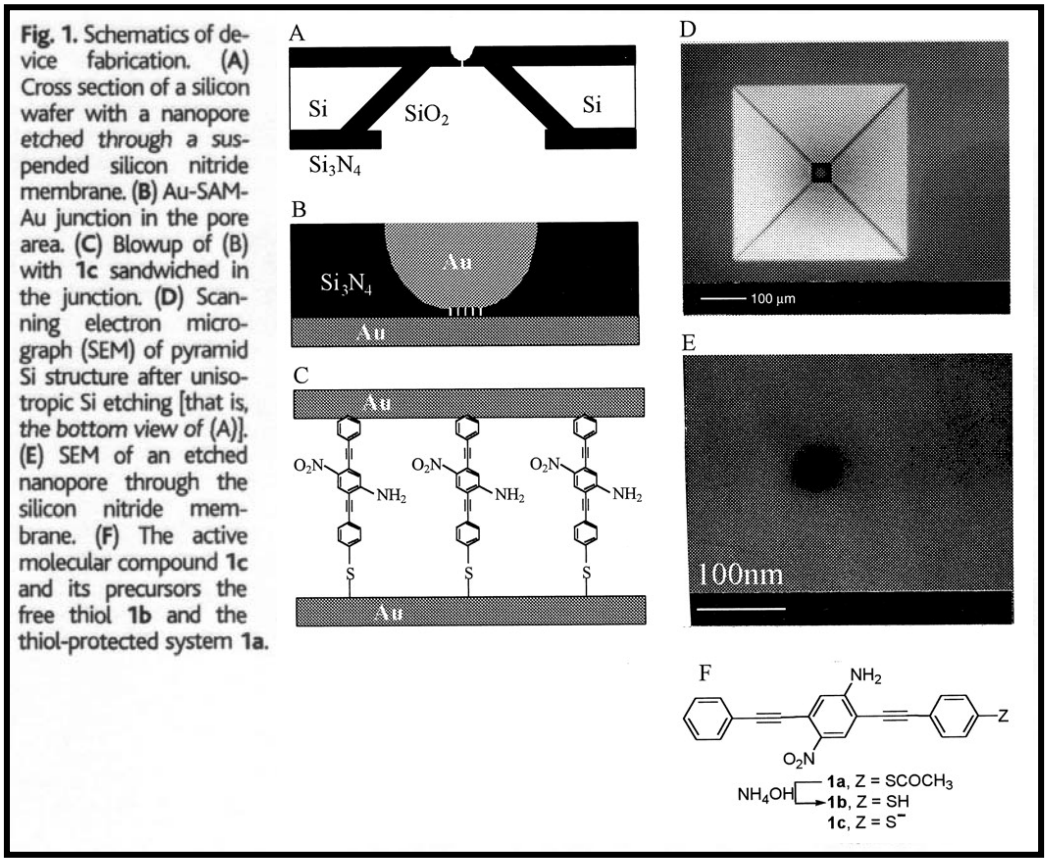


Fig. 1. Schematics of device fabrication. **(A)** Cross section of a silicon wafer with a nanopore *etched through a suspended* silicon nitride membrane. **(B)** Au-SAM-Au junction in the pore area. **(C)** Blowup of (B) with **1c** sandwiched in the junction. **(D)** Scanning electron micrograph (SEM) of pyramid Si structure after unisotropic Si etching [that is, *the bottom view of* (A)]. **(E)** SEM of an etched nanopore through the silicon nitride membrane. **(F)** The active molecular compound **1c** and its precursors the free thiol **1b** and the thiol-protected system **1a**.

J. Chen, *et al.*, *Science*, **286**, 1550 (1999).

Molecular Negative Differential Resistance

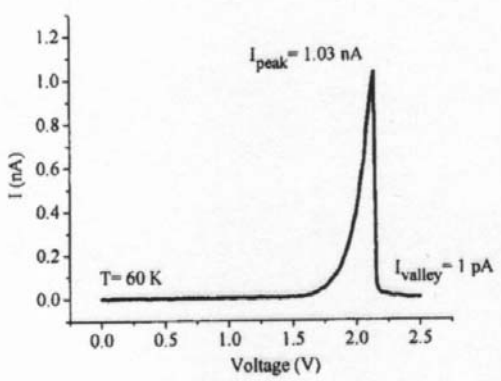


Fig. 2. *I*(*V*) characteristics of a Au-(2′-amino-4-ethynylphenyl-4′-ethynylphenyl-5′-nitro-1-benzenethiolate)-Au device at 60 K. The peak current density is ~50 A/cm², the NDR is ~−400 μohm cm², and the PVR is 1030:1.

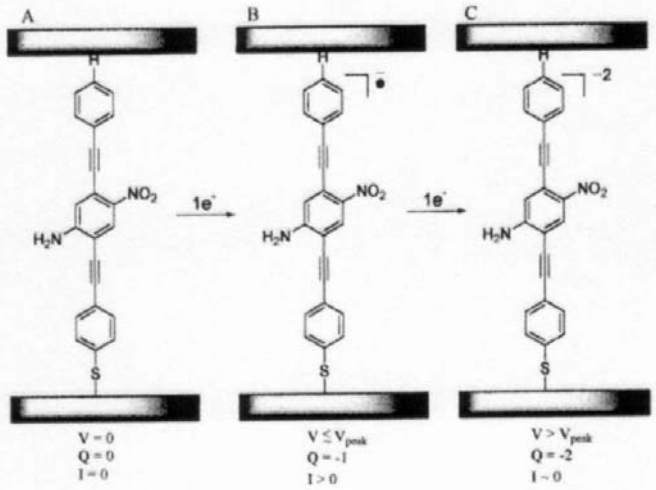
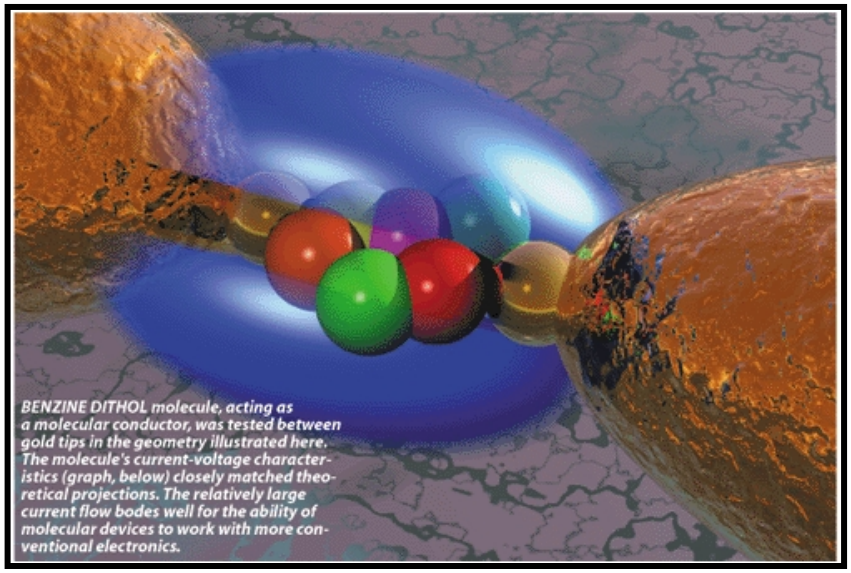


Fig. 4. Potential mechanism for the NDR effect. As voltage is applied, the molecules in the SAM (**A**) undergo a one-electron reduction to form the radical anion (**B**) that provides a conductive state. Further increase of the voltage causes another one-electron reduction to form the dianion insulating state (**C**). Q is the charge.

J. Chen, *et al.*, *Science*, **286**, 1550 (1999).

Recent Molecular Electronics Research

Metal-Molecule-Metal Junctions:



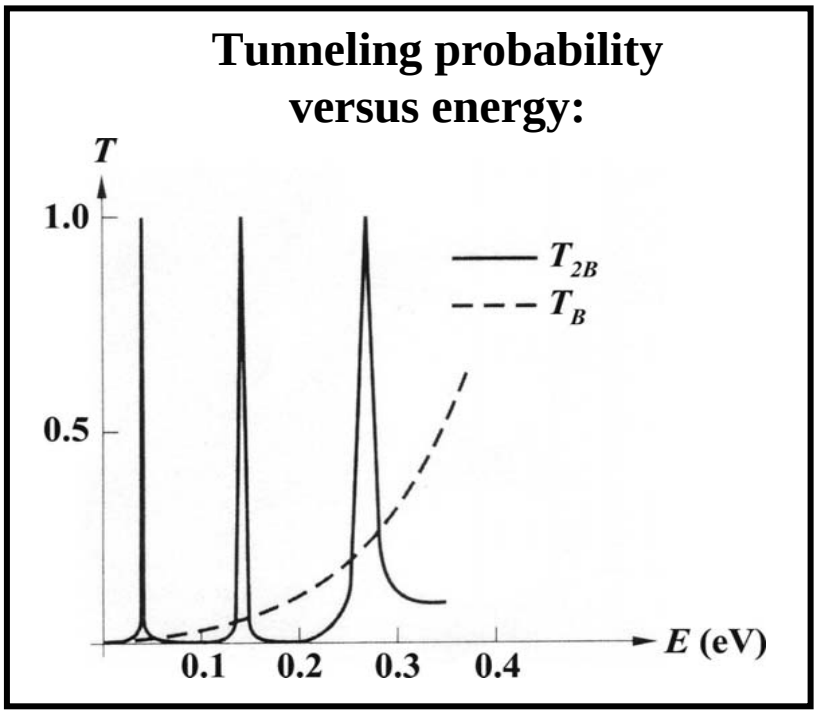
Sci. American, **282**, 86 (2000).

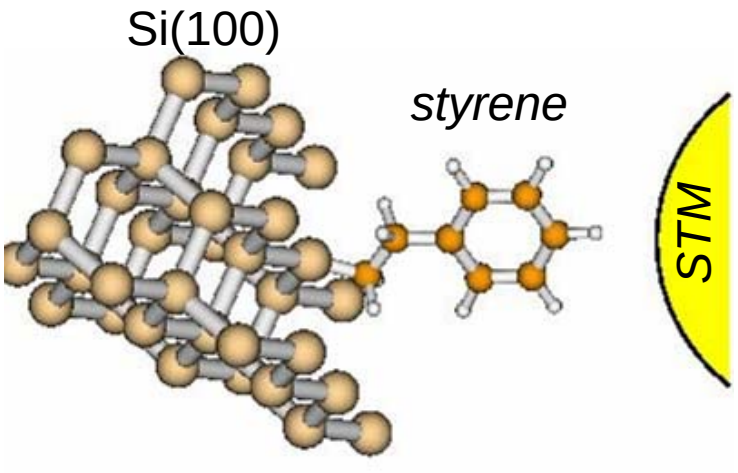
Recent results suggest that the contacts play a large – if not dominant role – in molecular electronic devices.

Science, **300**, 1384 (2003).

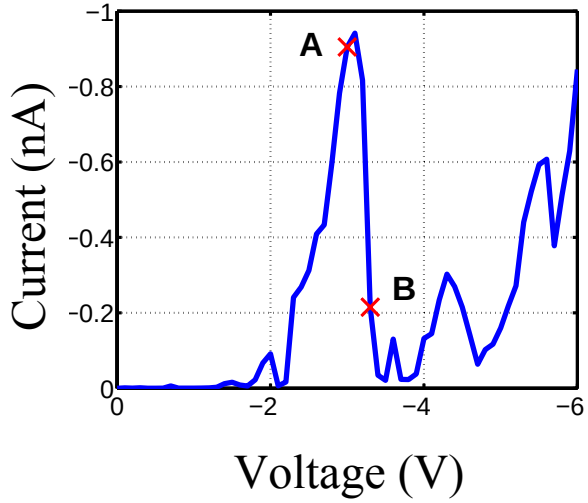
Semiconductor-Molecule-Metal Junctions

Molecular Resonant Tunneling Diode (RTD):
Negative Differential Resistance (NDR)

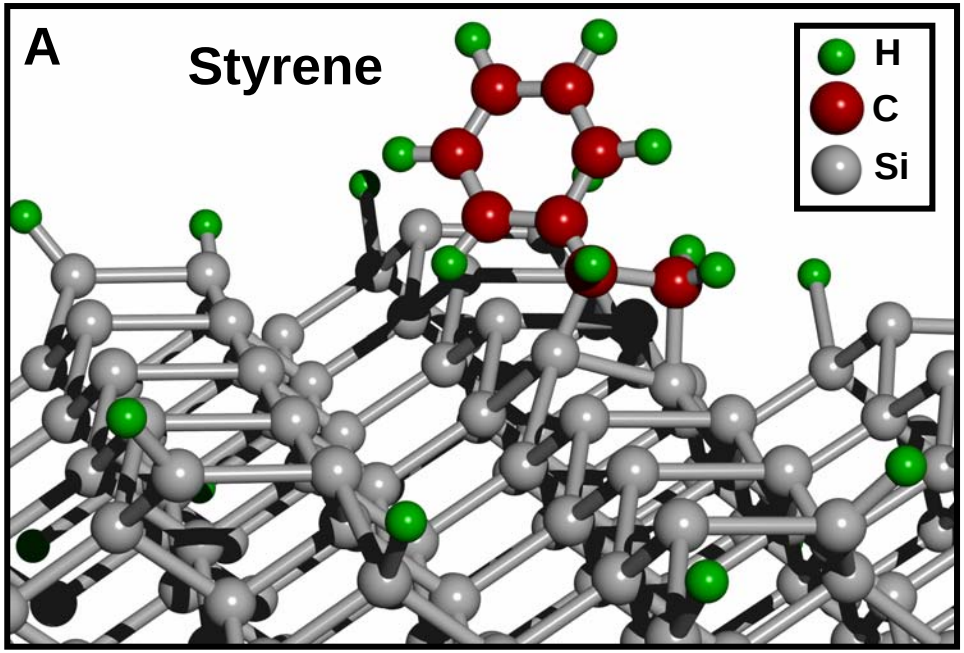


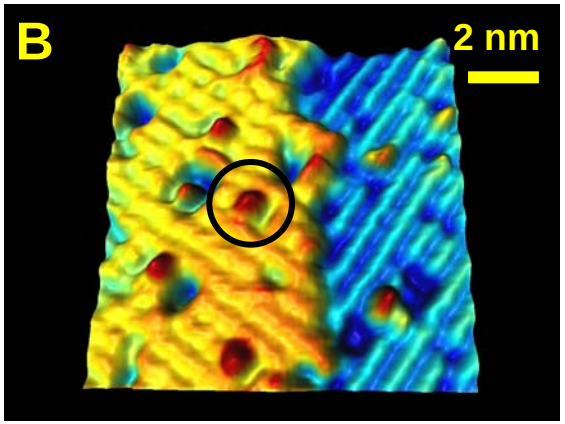


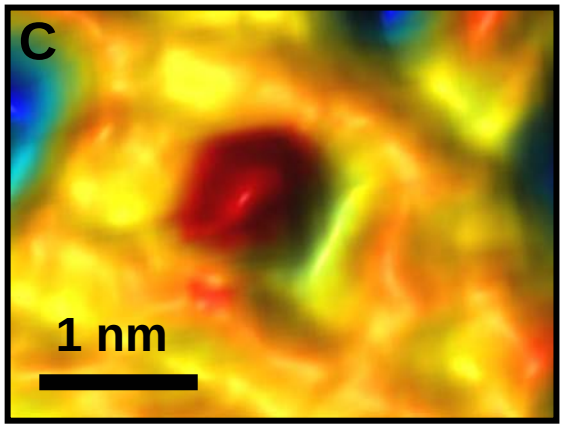
Calculated I-V Curve:



Styrene on the Si(100)-2×1 Surface



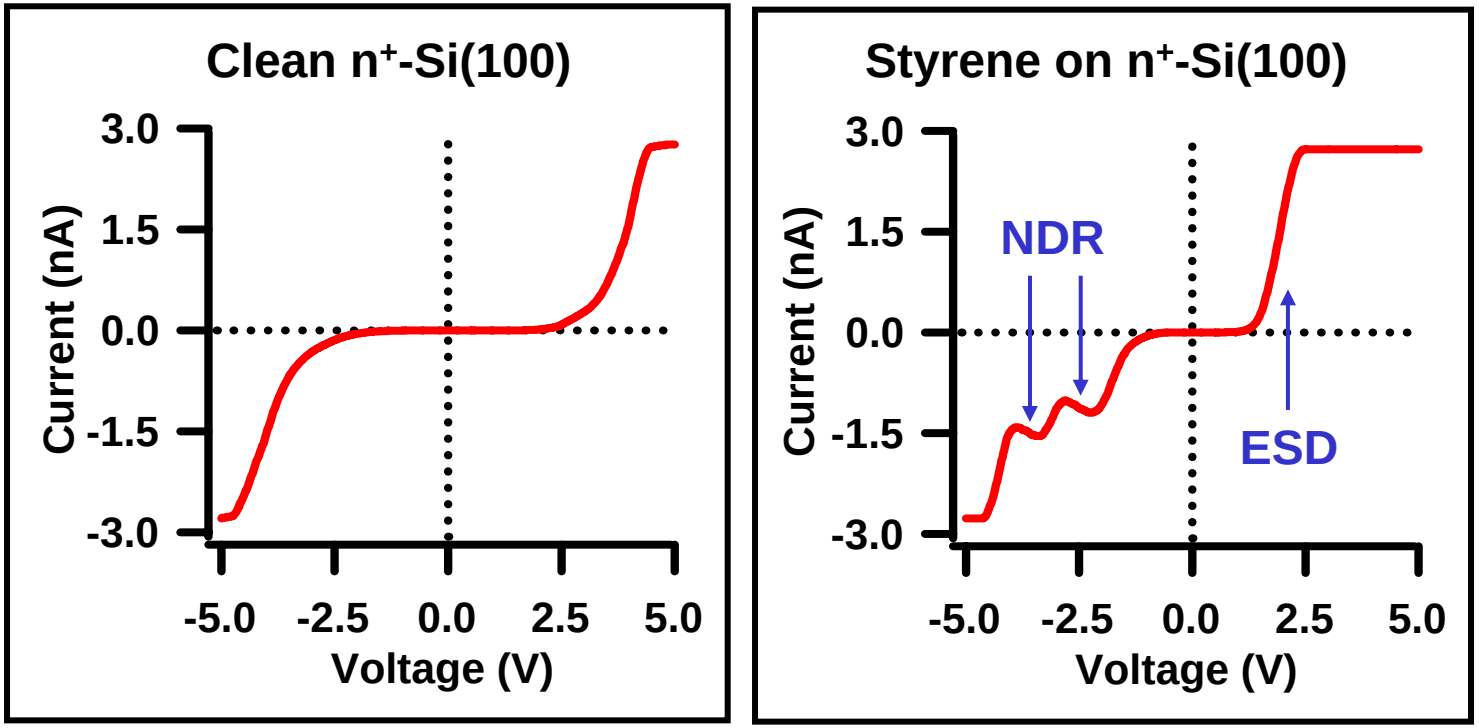




Individual styrene molecules are probed with the scanning tunneling microscope

N. P. Guisinger, *et al.*, *Nano Letters*, **4**, 55 (2004).

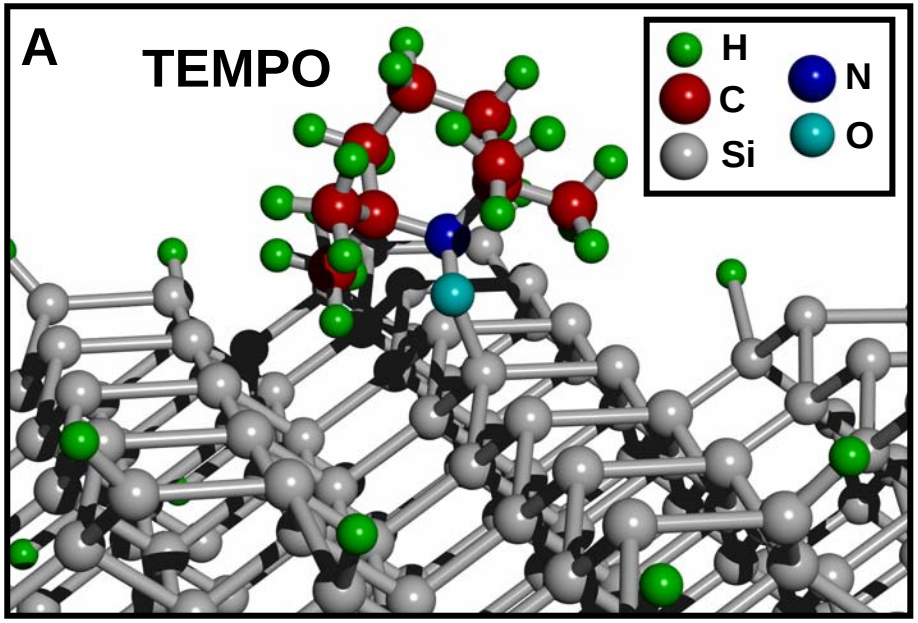
I-V Curve for Styrene on n^+-Si(100)

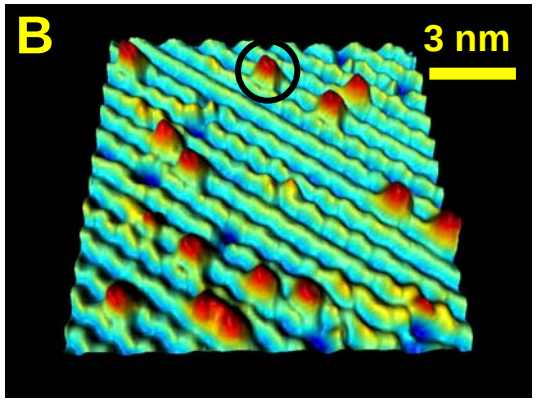


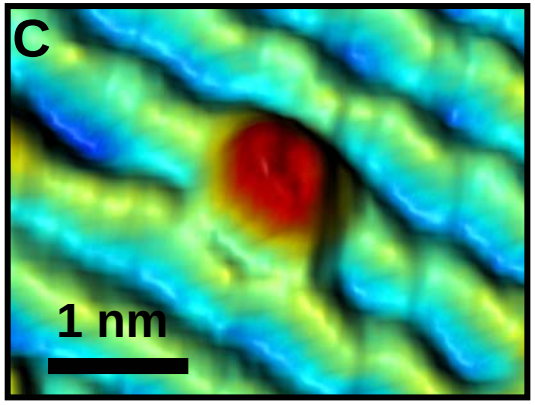
- Multiple NDR events.
- NDR is only observed at negative sample bias.
- Molecule is desorbed from the surface at positive bias.

TEMPO on the Si(100)-2×1 Surface

TEMPO:
(2,2,6,6-tetramethyl-1-piperidinyloxy)



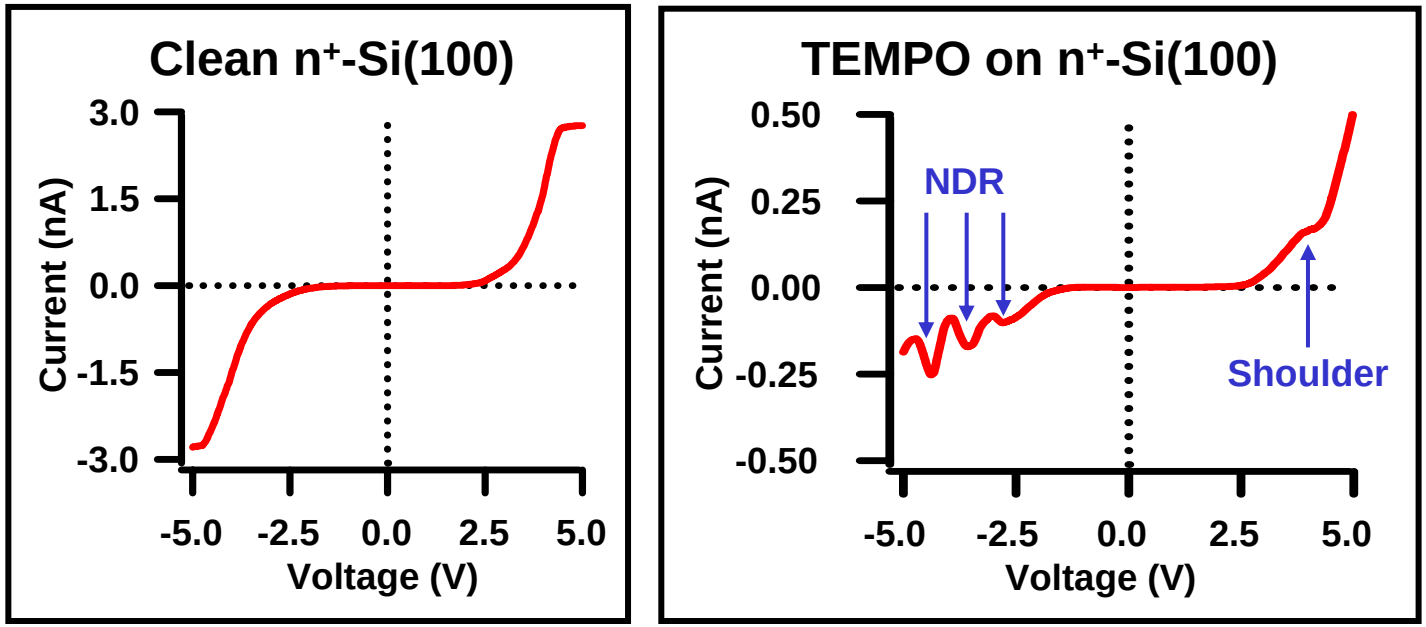




TEMPO resists electron stimulated desorption since it is a saturated hydrocarbon

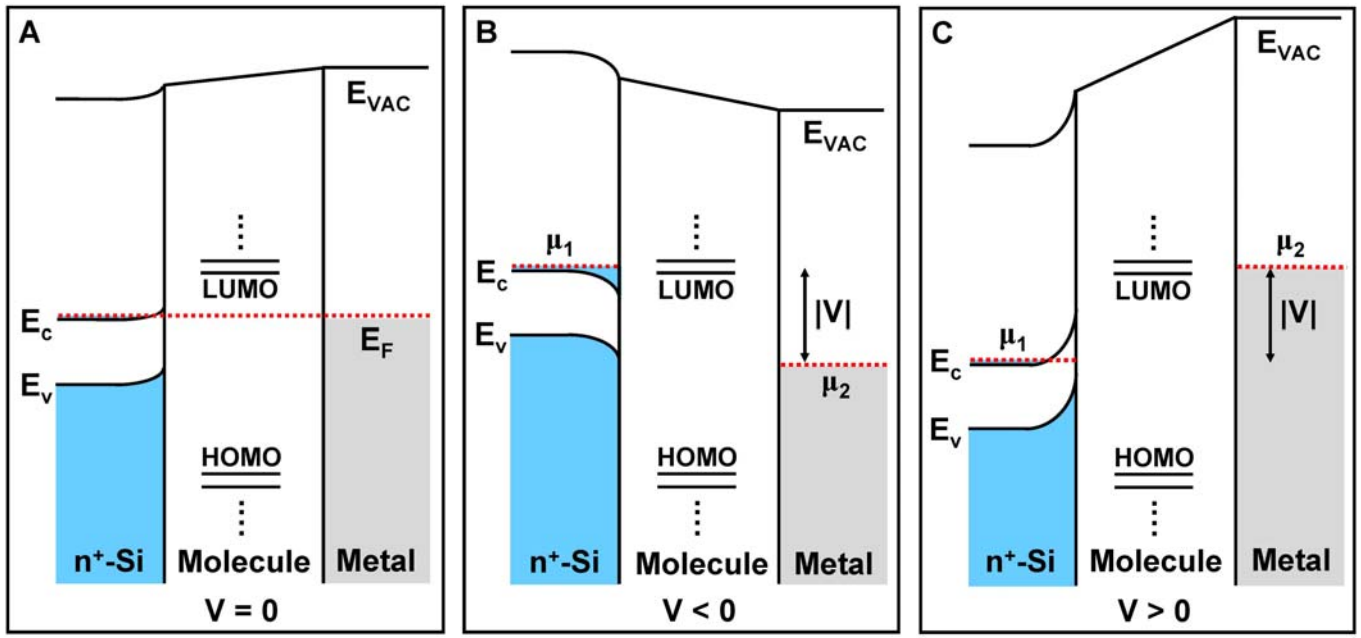
N. P. Guisinger, *et al.*, *Nano Letters*, **4**, 55 (2004).

I-V Curve for TEMPO on n^+-Si(100)



- Multiple NDR events.
- NDR is only observed at negative sample bias.
- Shoulder is only observed at positive sample bias.

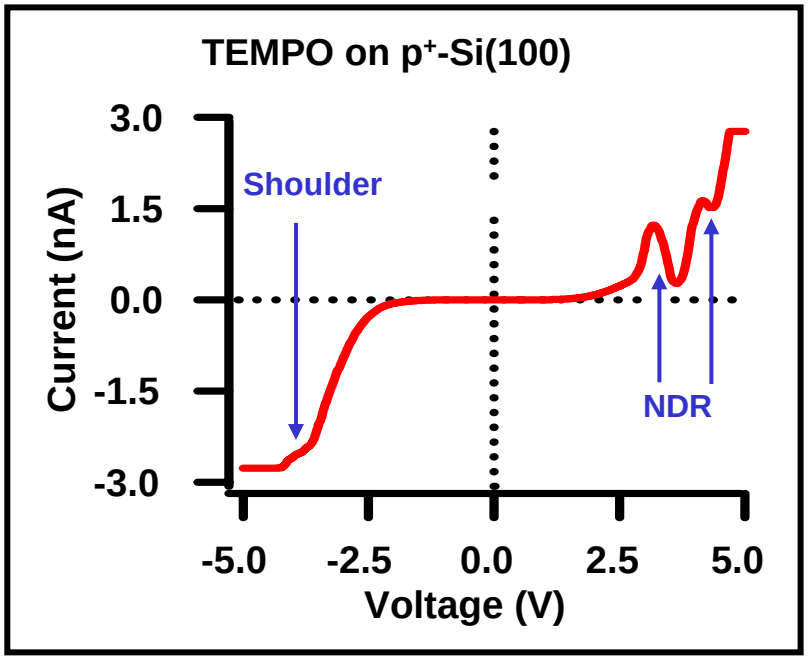
Band Diagrams for Molecules on n^+-Si(100)



Equilibrium **NDR** **Shoulder**

For p^+-Si(100), the behavior should be qualitatively the same, except at the opposite bias polarity.

NDR for TEMPO on p^+-Si(100)



- **Qualitatively similar behavior to TEMPO on n^+-Si(100) except opposite polarity, as expected.**

Molecular Electronics

To become commercially viable, many obstacles must be overcome:

(1) Macroscopic contacts, interconnections

(2) Integration with conventional devices

(3) Reliability

(4) Reproducibility

→ Defect tolerant architectures and nanotube electronics help circumvent some of these problems

A Defect-Tolerant Computer Architecture: Opportunities for Nanotechnology

James R. Heath, Philip J. Kuekes, Gregory S. Snider, R. Stanley Williams

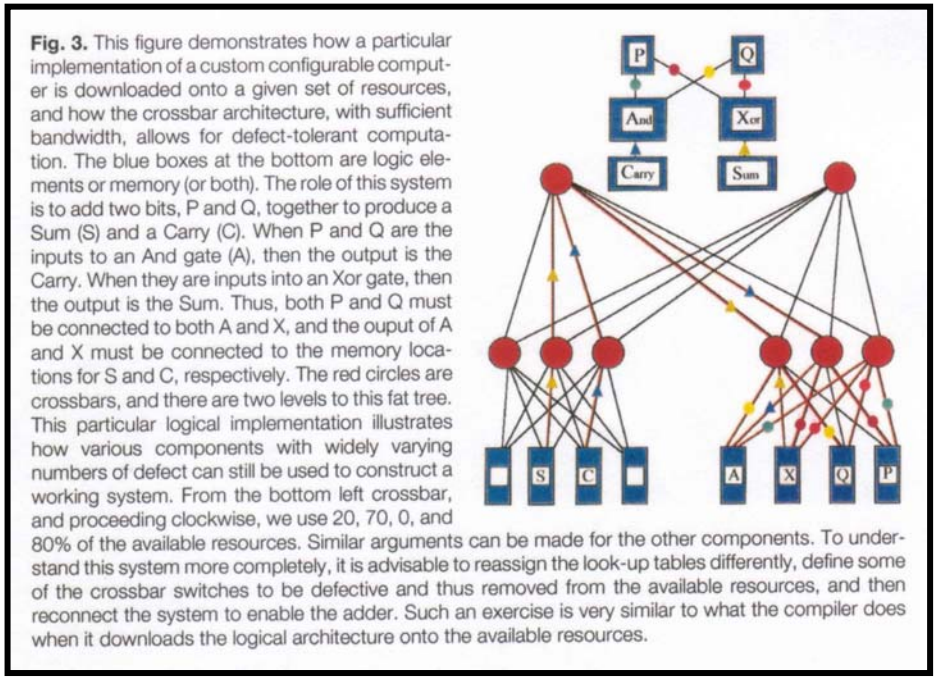
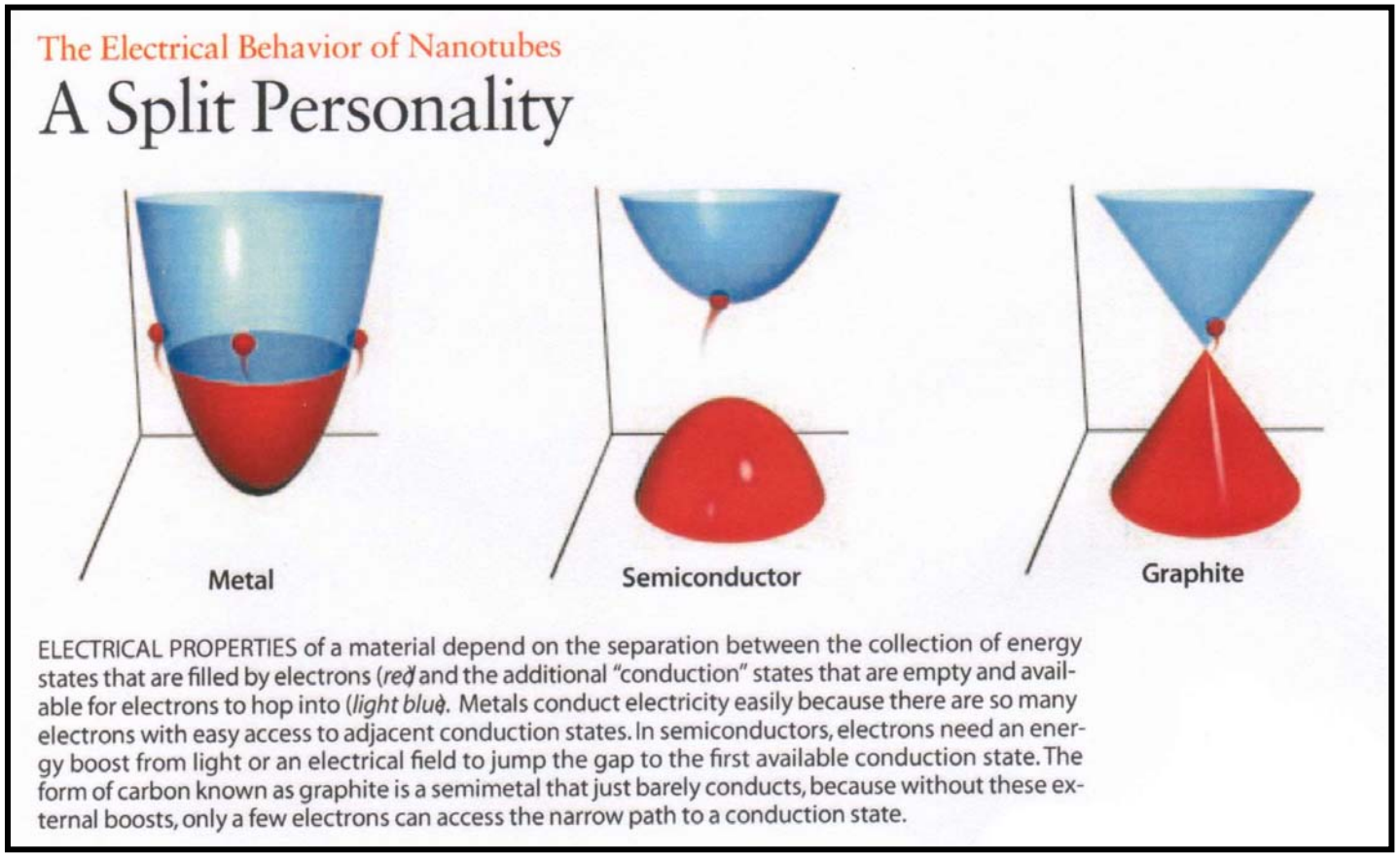


Fig. 3. This figure demonstrates how a particular implementation of a custom configurable computer is downloaded onto a given set of resources, and how the crossbar architecture, with sufficient bandwidth, allows for defect-tolerant computation. The blue boxes at the bottom are logic elements or memory (or both). The role of this system is to add two bits, P and Q, together to produce a Sum (S) and a Carry (C). When P and Q are the inputs to an And gate (A), then the output is the Carry. When they are inputs into an Xor gate, then the output is the Sum. Thus, both P and Q must be connected to both A and X, and the ouput of A and X must be connected to the memory locations for S and C, respectively. The red circles are crossbars, and there are two levels to this fat tree. This particular logical implementation illustrates how various components with widely varying numbers of defect can still be used to construct a working system. From the bottom left crossbar, and proceeding clockwise, we use 20, 70, 0, and 80% of the available resources. Similar arguments can be made for the other components. To understand this system more completely, it is advisable to reassign the look-up tables differently, define some of the crossbar switches to be defective and thus removed from the available resources, and then reconnect the system to enable the adder. Such an exercise is very similar to what the compiler does when it downloads the logical architecture onto the available resources.

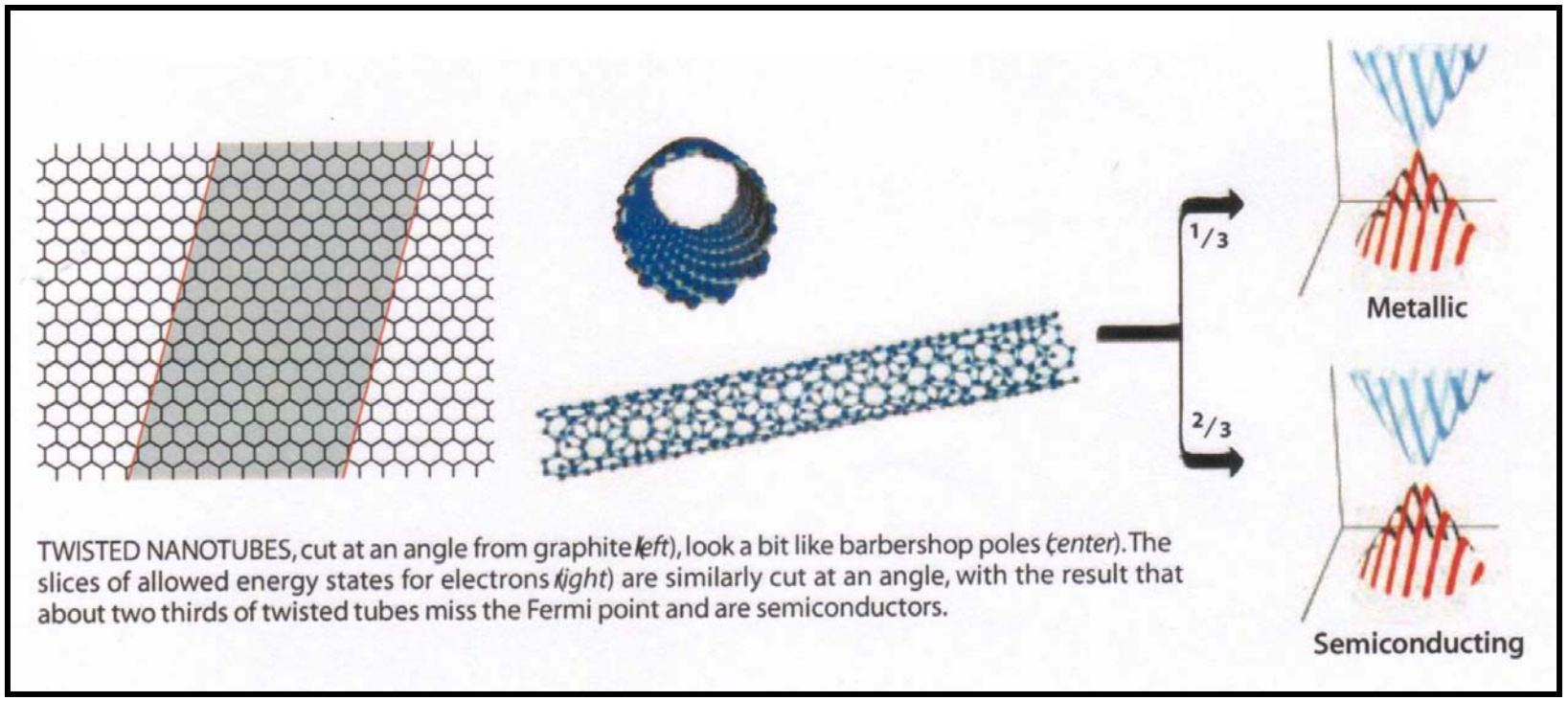
J. R. Heath, *et al.*, *Science*, **280**, 1716 (1998).

Electrical Properties of Graphite



P. G. Collins and Ph. Avouris, *Scientific American*, **283**, 62 (2000).

Electrical Properties of Nanotubes



TWISTED NANOTUBES, cut at an angle from graphite (*left*), look a bit like barbershop poles (*center*). The slices of allowed energy states for electrons (*right*) are similarly cut at an angle, with the result that about two thirds of twisted tubes miss the Fermi point and are semiconductors.

P. G. Collins and Ph. Avouris, *Scientific American*, **283**, 62 (2000).

Nanotube Complementary Logic - Doping

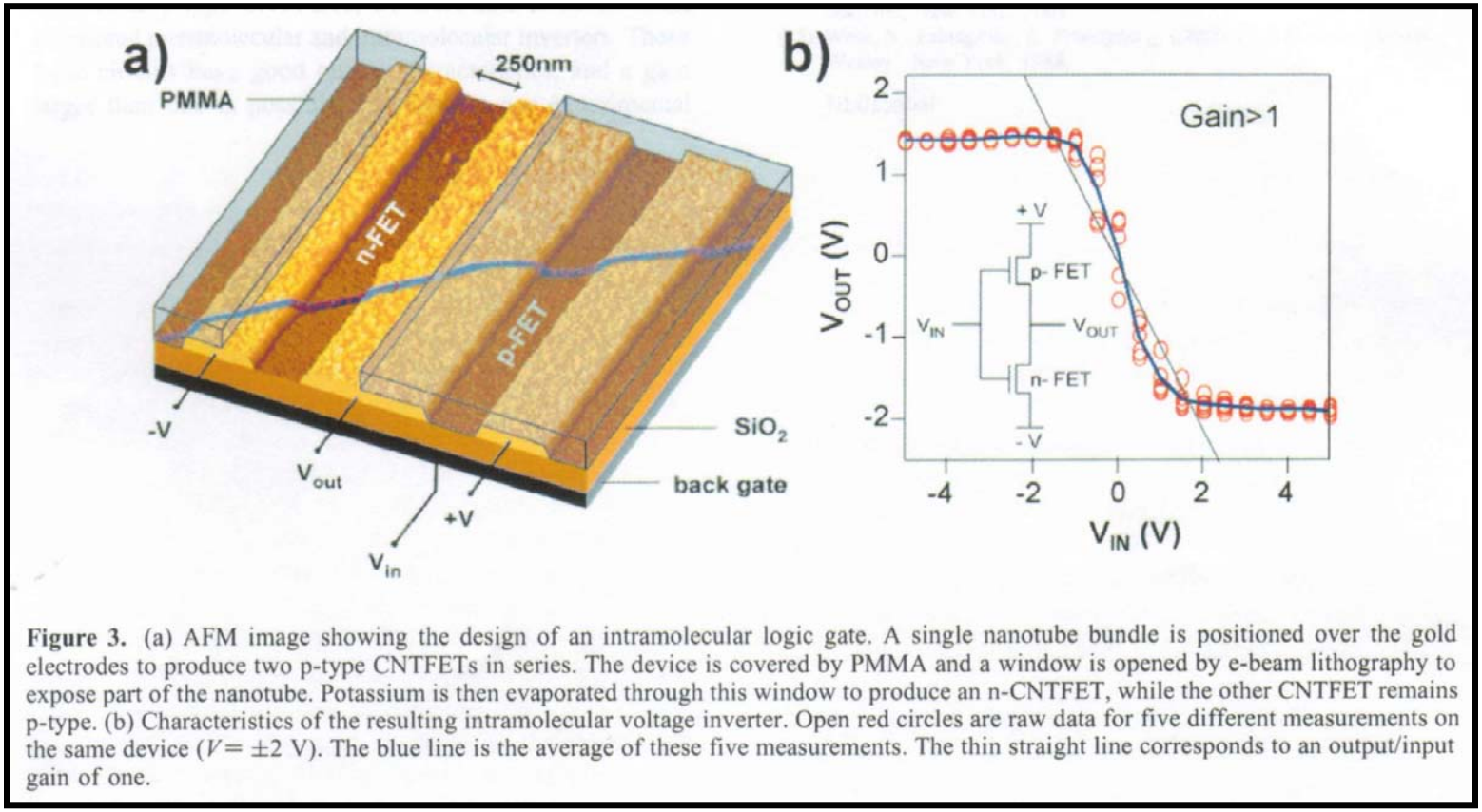
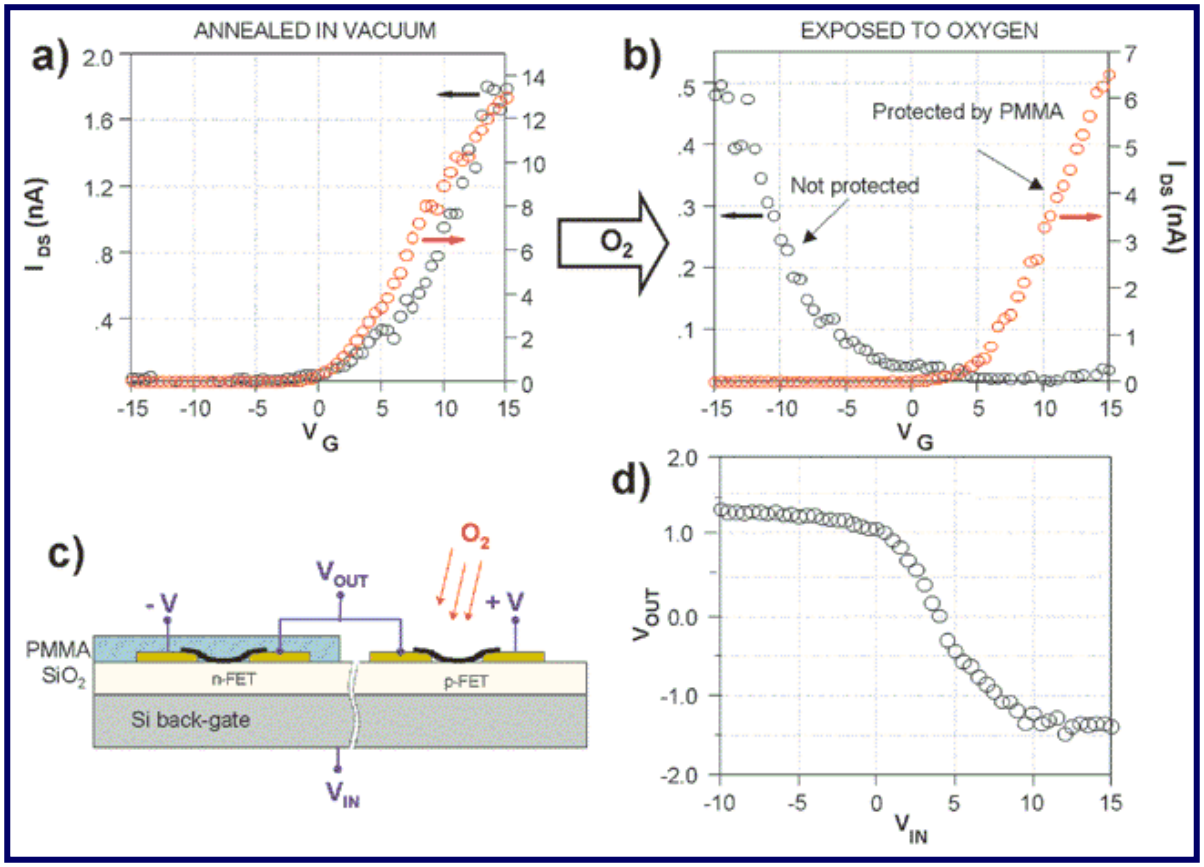


Figure 3. (a) AFM image showing the design of an intramolecular logic gate. A single nanotube bundle is positioned over the gold electrodes to produce two p-type CNTFETs in series. The device is covered by PMMA and a window is opened by e-beam lithography to expose part of the nanotube. Potassium is then evaporated through this window to produce an n-CNTFET, while the other CNTFET remains p-type. (b) Characteristics of the resulting intramolecular voltage inverter. Open red circles are raw data for five different measurements on the same device ($V = \pm 2$ V). The blue line is the average of these five measurements. The thin straight line corresponds to an output/input gain of one.

V. Derycke, *et al.*, *Nano Letters*, **1**, 453 (2001).

Nanotube Complementary Logic - Annealing



V. Derycke, *et al.*, *Nano Letters*, **1**, 453 (2001).

Ambipolar Carbon Nanotube FET

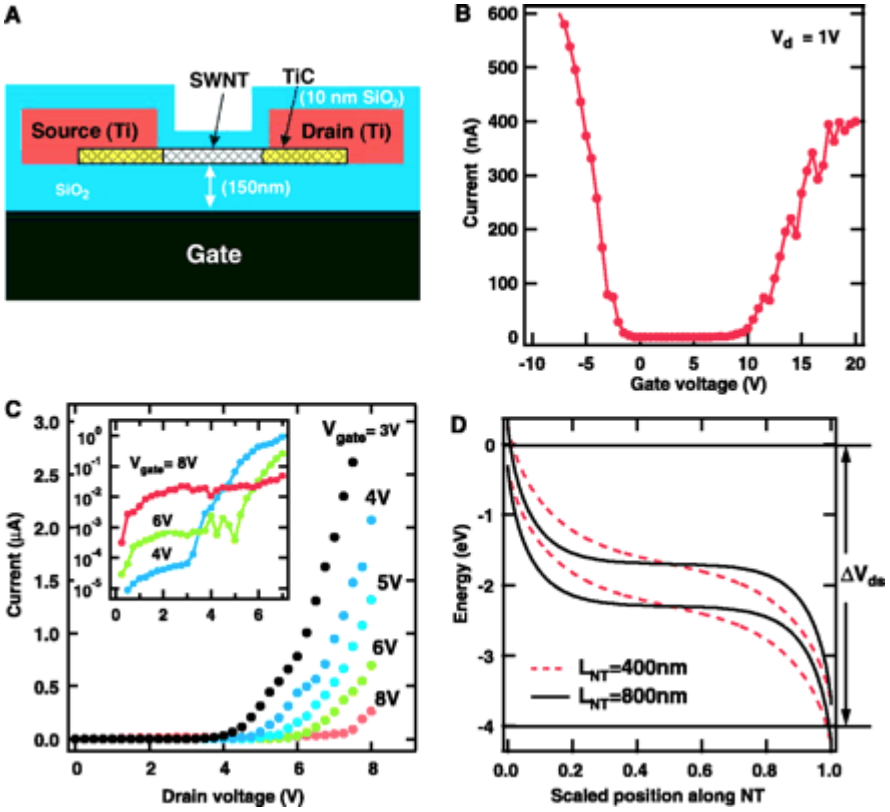


Fig. 1. (**A**) Schematic diagram of the ambipolar s-SWNT device structure. (**B**) Electrical characterization of a typical ambipolar device. A plot of the drain current versus *V*g for a grounded source and a small drain potential of1Vis shown. The data indicate ambipolar behavior. (**C**) Plot of the drain current versus *V*d for a grounded source and a gate potential of 5 V for the device used in the optical measurements. The inset shows the data on a logarithmic scale. (**D**) Calculated band structure for carbon nanotube FET devices with *V*d = 4 V and *V*g halfway between the source and drain voltages.

J. A. Misewich, *et al.*, *Science*, **300**, 783 (2003).

Infrared Emission from an Ambipolar Nanotube FET

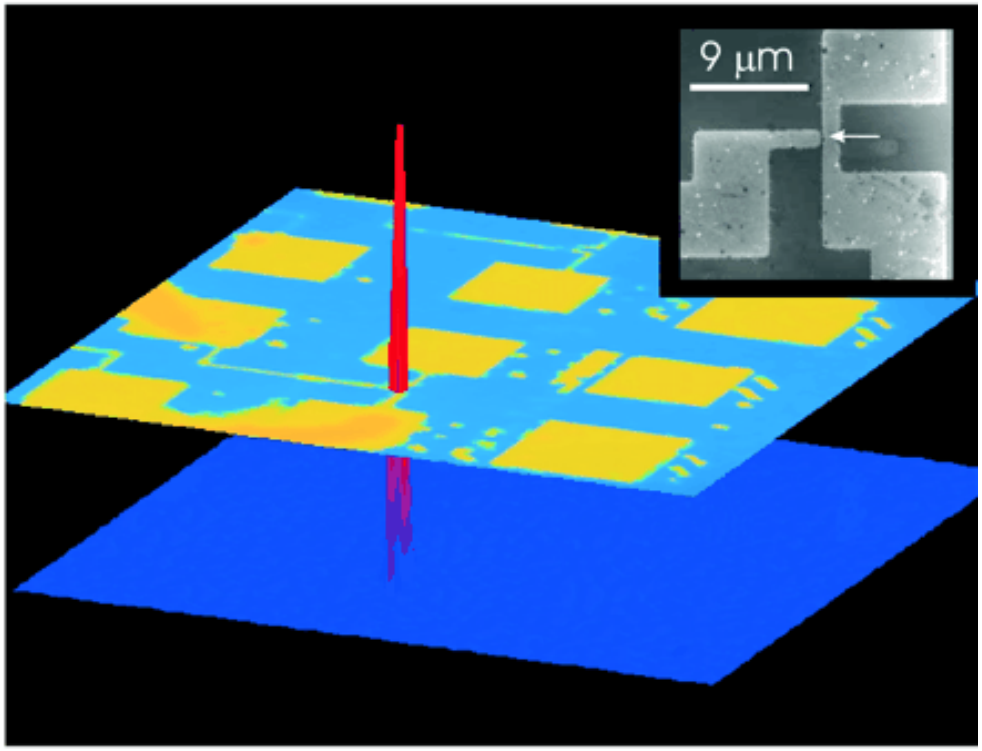
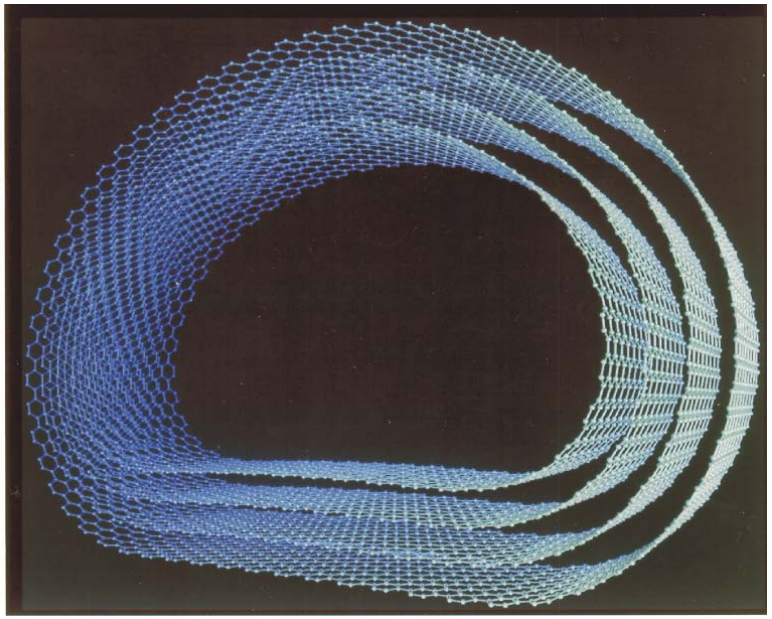


Fig. 2. Optical emission from an ambipolar carbon nanotube FET detected with an IR camera. The upper plane is a color-coded IR image of the carbon nanotube FET. The contact pads and thin wires leading to the carbon nanotube channel are shown in yellow. The lower plane is the surface plot of the IR emission image taken under conditions of simultaneous e– and h+ injection into the carbon nanotube. The emission was localized at the position of the carbon nanotube. (**Inset**) SEM showing the device structure in the region of the nanotube emitter.

J. A. Misewich, *et al.*, *Science*, **300**, 783 (2003).

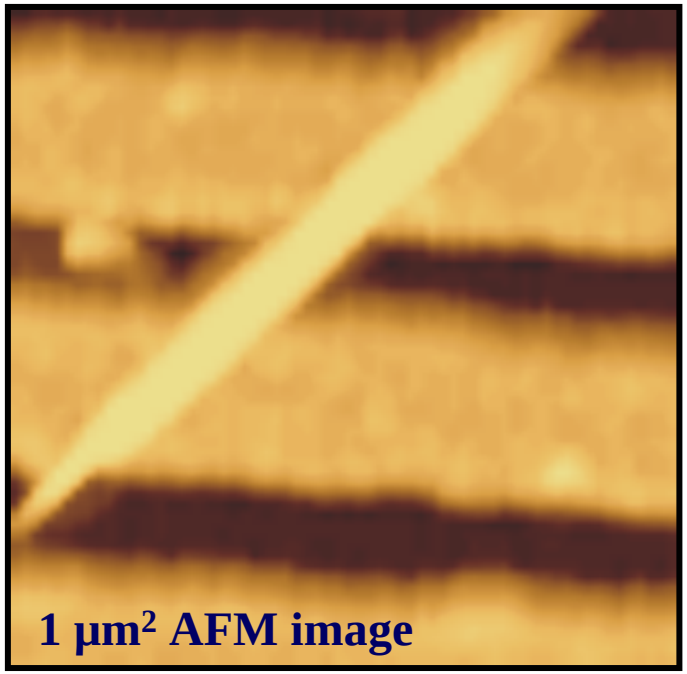
Electrical Properties of MWNTs



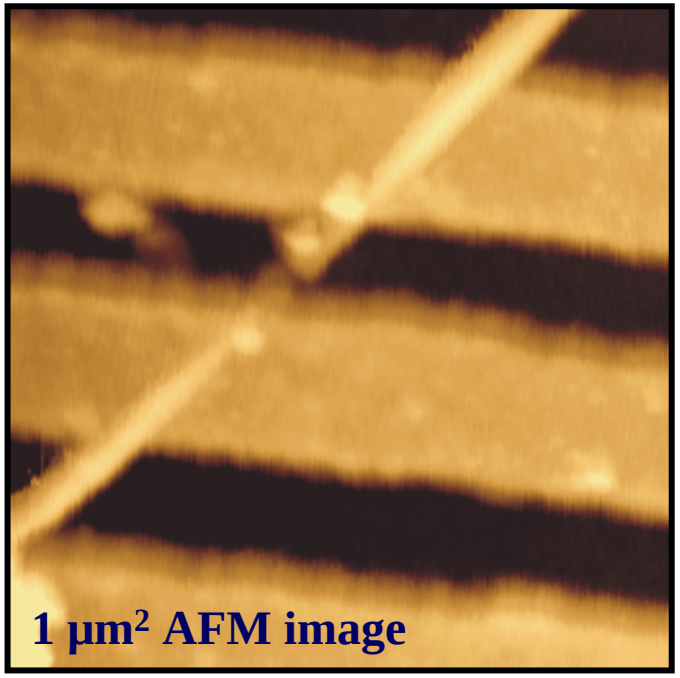
- MWNT bandgap is proportional to 1/d → At room temperature, MWNTs behave like metals since d ~ 10 nm
- Only the outermost shell carries current in an undamaged MWNT

Electrically Stressed MWNTs

Before Electrical Stress

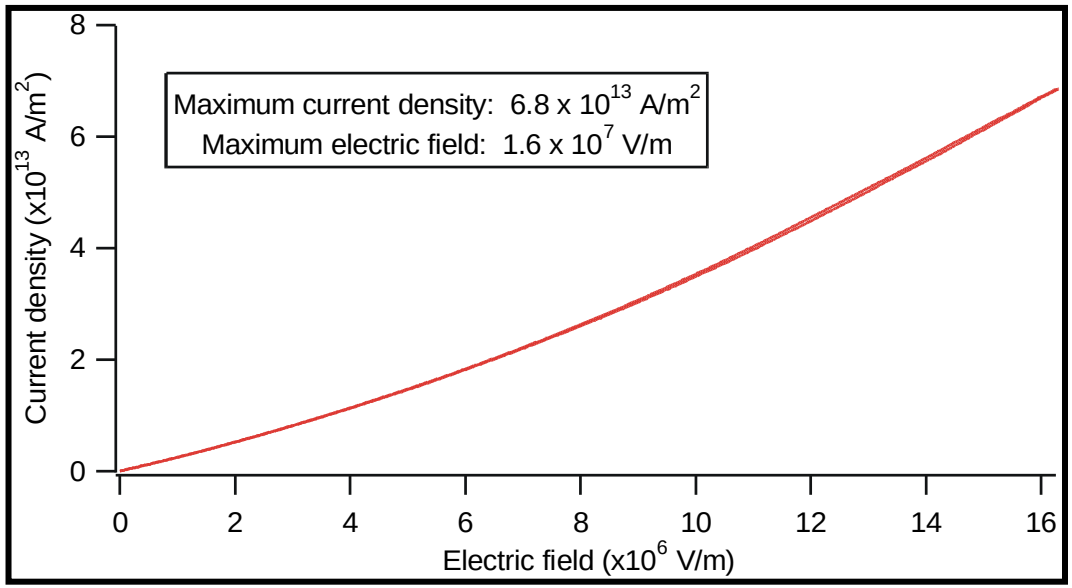


After Failure



Experimental method: Monitor the current as a function of time while stressing the MWNT at a fixed voltage.

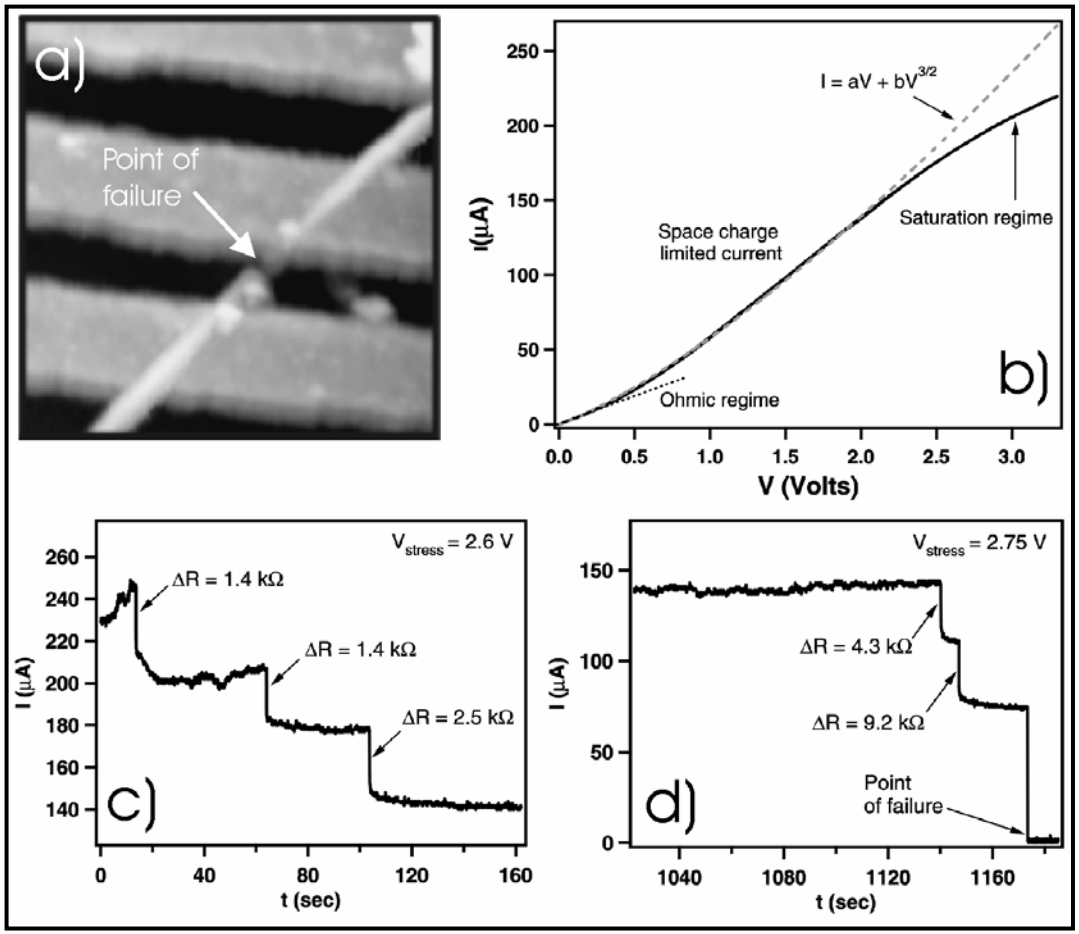
Representative MWNT I-V Curve:



Maximum current densities of potential interconnect materials:

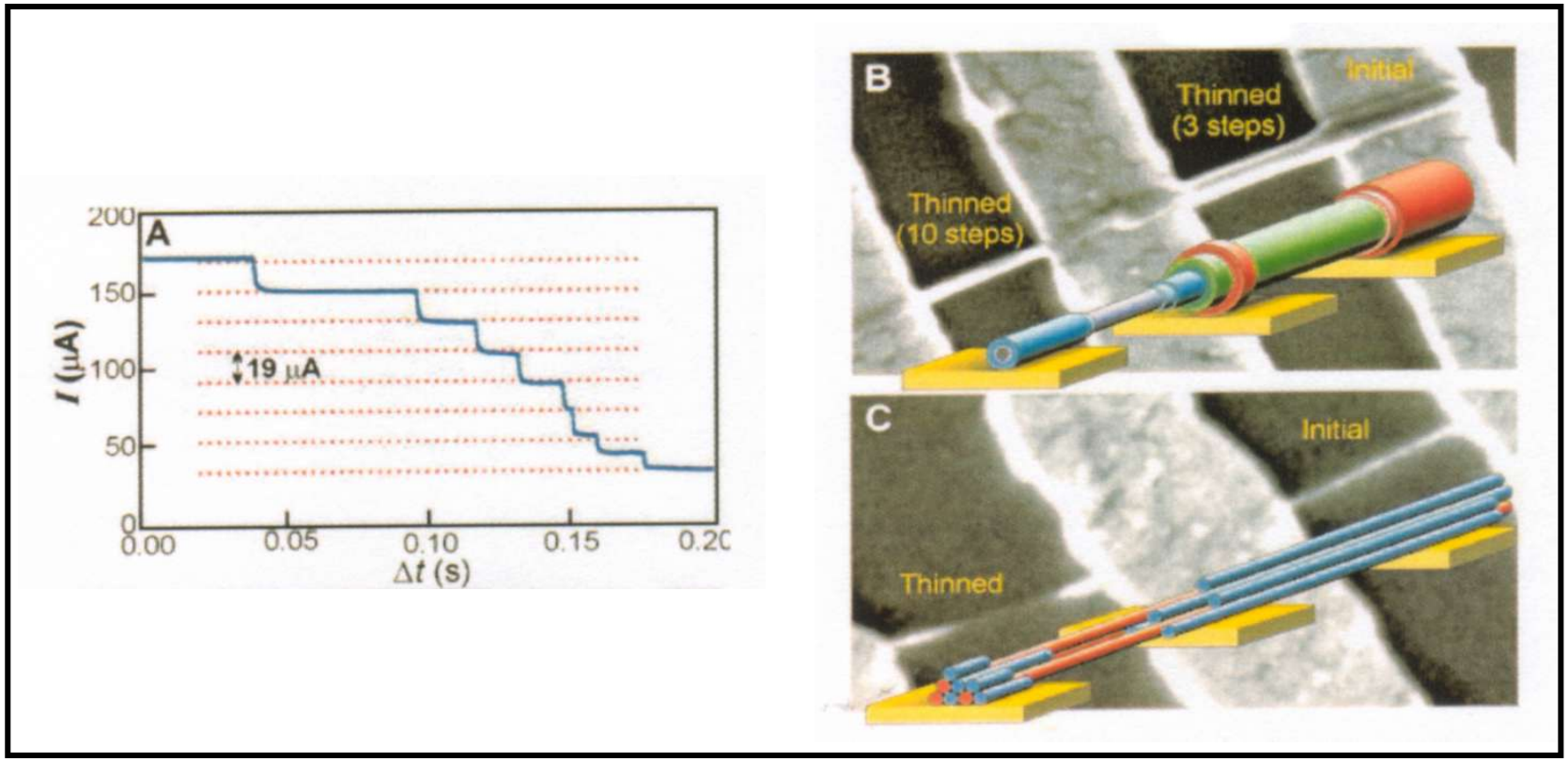
- Metals: $10^{10} – 10^{12}$ A/m^2
- Superconductors: $J_c \sim 10^{12}$ A/m^2
- MWNTs: >5×1013 A/m^2

Multiwalled Carbon Nanotube Failure



P. G. Collins, M. C. Hersam, M. Arnold, R. Martel, and Ph. Avouris, *Phys. Rev. Lett.*, 86, 3128 (2001).

Engineering Carbon Nanotubes Using Electrical Breakdown



P. G. Collins, *et al.*, *Science*, **292**, 706 (2001).

Engineering Carbon Nanotube Circuits Using Electrical Breakdown

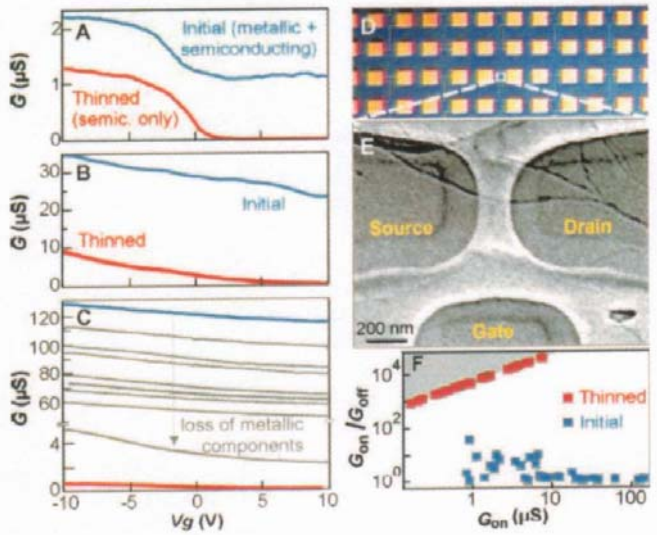


Fig. 4. (**A** and **B**) Stressing a mixture of s- and m-SWNTs while simultaneously gating the bundle to deplete the semiconductors of carriers resulted in the selective breakdown of the m-SWNTs. The $G(V_g)$ curve rigidly shifted downward as the m-SWNTs were destroyed. The remaining current modulation is wholly due to the remaining s-SWNTs. (**C**) In very thick ropes, some s-SWNTs must also be sacrificed to remove the innermost m-SWNTs. By combining this technique with standard lithography, arrays of three-terminal, nanotube-based FETs were created (**D** and **E**) out of disordered bundles containing both m- and s-SWNTs. Although these bundles initially show little or no switching because of their metallic constituents, final devices with good FET characteristics were reliably achieved (**F**).

Table 1. Comparison of relative band gaps from experiments (Fig. 2B) with calculations based on the expected diameter dependence. The only parameters are the initial diameter of the tube and the 0.34 nm spacing between adjacent shells. Calc., calculated; Meas., measured.

Shell	Diameter (nm)	Relative band gap (eV)	
		Calc.	Meas.
n	9.5		
~	~		
n-10	2.7	0.24	0.22
n-11	2.0	0.33	
n-12	1.3	0.49	0.48
n-13	0.7	1.00	1.00

P. G. Collins, *et al.*, *Science*, **292**, 706 (2001).